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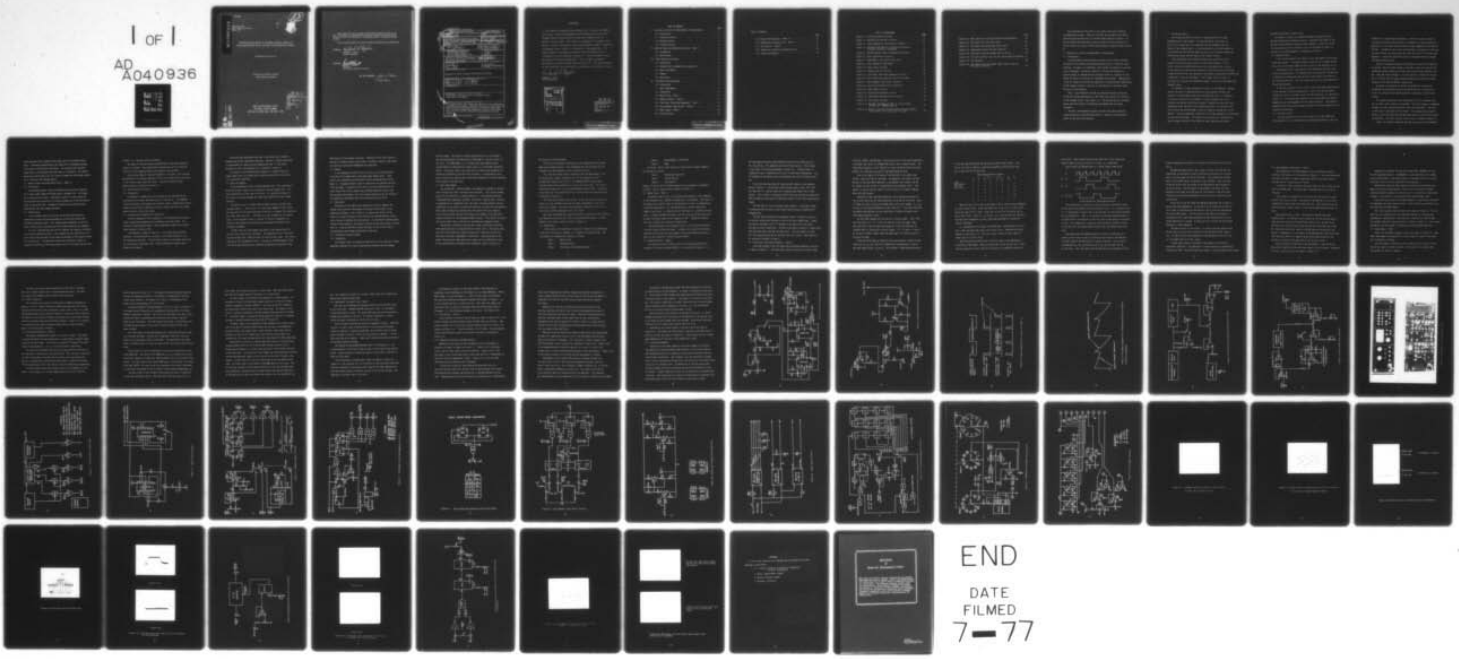

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Final Technical Report
March 1977

INVESTIGATION AND DESIGN OF ELECTRONIC CIRCUITRY RELATED TO NOISE AND RADIATION EFFECTS FOR SOLID STATE DEVICES AND CIRCUITS

Northeastern University

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This report details the design and operation of four different instrumentation systems. These are circuitry for evaluating the charge and discharge characteristics of Schottky diode detectors, an optical signal and random noise source, noise reduction circuitry and an IR detector three phase CCD scanning system.

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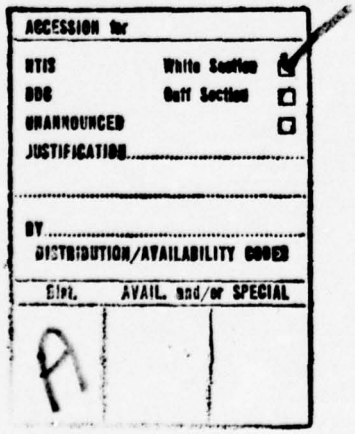
EVALUATION

1. This effort has produced several original state of the art instrumentation systems. The first demonstration of IR Schottky barrier stare and integrate mode of operation used the charge and discharge circuit of Section I in this report. This circuit is recommended for candidate video sensors. Section II describes a unique signal generator capable of supplying low frequency optical signals in the presence of fast gamma noise. The signal generator was necessary to properly test and evaluate the noise circumvention circuits described in Section III. The circumvention circuit was capable of 25 db noise suppression. The most complex instrument developed was the IRCCD scanning system in Section IV. This system operates at near theoretical noise levels and is outstanding in all aspects of design.

Richard W. Taylor

RICHARD W. TAYLOR
Project Engineer



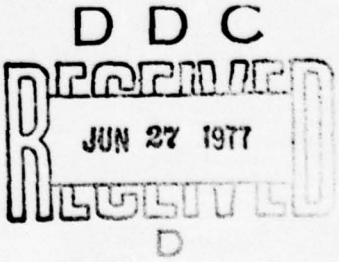


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TABLE OF CONTENTS

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Table of Contents

LIST OF ILLUSTRATIONS

The investigations described in this report cover four different instrumentation systems. These are circuitry for evaluating the charge and discharge characteristics of Schottky diode detectors, Section I, An Optical Signal and Random Noise Source, Section II, noise reduction circuitry, Section III and an IR three phase detector scanning system, Section IV.

I. Electronic Circuitry for Measurement of Charge Decay

1.0 Introduction

The investigation requiring the circuitry of this section involved evaluation of the charge and discharge characteristics of Schottky diode detectors. By means of a mechanical light shutter the detector is periodically illuminated. During the "black out" interval the detector is reverse biased, or charged and the resultant current is a measure of the amount of charge lost during the illuminated time interval. Additionally, it was of interest to provide the capability of evaluating the significance of the leakage current in terms of its contribution to the decay characteristics of the detector.

Thus, it was decided to provide two charging intervals during the "black out" period separated by a sufficient time interval for evaluation of the leakage current. (see Figure 1.3.) The detector must be isolated during the entire time of illumination and between the two charge intervals.

The basic instrumentation system is broken into three functions; timing and control, charging and isolation. These will be described in detail in the next three sections.

1.1 Timing and Control

The timing and control circuitry is synchronized with a signal generated by the light shutter. For this particular application it was a 10 volt square wave at a frequency that was dependent upon the speed of light chopping wheel. A two stage amplifier with the capability of adjusting the amplitude and phase was used as an interface between the synchronizing signal and the input to the timing circuitry.

Three monostable multivibrators connected in cascade are used to generate the necessary gating pulses in the proper sequence. In the initial design three NE555 timers were used to implement this circuitry. In the interest of reducing the complexity of the circuitry and minimizing triggering difficulties the second and final design incorporated an SN74123 and an SN74L122 in place of the NE555's. This design, shown in Figure 1.1, used fewer IC's and passive components; however, the current requirement was somewhat higher.

The SN74123 is a dual monostable circuit as is the SN74L122. Neither require any special triggering waveform as they operate on either the leading or trailing edge of the input synchronizing pulse. As indicated in Figure 1.2 one half of the SN74123 is used to generate the initial charging time interval control pulse which is nominally 20 usec and occurs immediately after the end of the illumination period. At the end of the 20 usec pulse the trailing edge is used to trigger the second unit of the SN74123. This unit generates a delay that is variable between 2.5 milliseconds to about 20 milliseconds. The output of this second unit, following the delay, triggers one half of the SN74L122, which generates the second

charging time interval control pulse.

An OR gate is used as an interface between the timing circuitry and the charging and isolation circuitry. Originally the output of the OR gate controlled both of these circuits; however, in the final design it was used only for the isolation circuit as indicated in Figure 1.2. Details of the timing sequence is indicated in Figure 1.3.

1.2 Charging Circuit

In the initial design of the charge circuit the output of the OR gate served two purposes. The output served as the input to a control gating circuit for the isolation amplifier and an input to the charging circuit.

The charging circuit consisted of a 531 operational amplifier used in the noninverting mode. The voltage level of the output of the OR gate is amplified to the desired level by the 531 and serves as one input to the isolation amplifier. Thus, the charge amplifier was synchronized with the two charge pulses.

In the final version of this circuit it was found that synchronization of the charging circuit was unnecessary. Instead, the desired charge voltage was fixed at the input of the isolation amplifier, as indicated in Figure 1.2. A 741 operational amplifier with variable gain and internal compensation was found adequate for the charge amplifier. This approach, nonswitching of the charging voltage, resulted in reduced compensation and transient difficulties.

1.3 Isolation Circuit

The basic operation of this circuit makes use of the sample and hold capabilities of an operational-transconductance amplifier, OTA, and

a MOS-FET in a closed loop configuration. The OTA is unique in that it is capable of being strobed such that it operates as a normal operational amplifier or is off with zero gain with an output impedance of the order of 10^9 ohms. The MOS-FET used in the source-follower configuration closes the loop and isolates the device under test, DUT, by virtue of its large input impedance. Closed loop operation results in improved transient response and reduced charging time.

The DUT is connected between the OTA output, the gate of the MOS-FET, and ground. When the stobe voltage to the OTA is zero volts the OTA and the MOS-FET operate normally with the input charge voltage applied to the DUT. When the strobe voltage is -15 volts the OTA is turned off and the DUT is isolated from the charge voltage shunted by the output and input impedance of the OTA and MOS-FET respectively.

The decay of the charge of the DUT is obtained at the source of the MOS-FET source-follower without disturbing the DUT. An evaluation of the lost charge can be made by means of a resistance in series with the DUT.

The strobe voltage must have a magnitude of 15 volts, between zero and -15 volts, with a width or 20 useconds. This gate voltage is generated by means of a two stage discrete BJT circuit using two PNP's. The input to this gate is the output of the OR gate. This approach was necessary because of the pulse width and the amplitude which is difficult for normal IC amplifiers. The final version of this circuit is shown in Figure 1.2.

Figure 1.4 indicates waveforms obtained at the source of the MOS-FET

source-follower with a Schottky diode under test for different charge levels. Discharge characteristics for diode while illuminated and when in the dark are significantly different. The reverse biased junction charge decay is the greatest when the diode is illuminated. The smaller decay occurs during black out, the interval between the two charges pulses, and is related to the leakage current.

II. Optical Signal and Random Noise Source - Model II

2.0 Introduction

The prototype Optical Signal and Random Noise Source was reported on in report number AFCRL-TR-74-0058 dated 1 December 1973. This model had a fixed polarity output, a mechanical vernier for fine control of the noise PMT and no provision for external modulation of the LED optical input to the optical PMT. Subsequent evaluation has revealed certain modifications that were deemed desirable.

2.1 Modifications

In the original model fine control of the noise PMT output was obtained by varying the spacing between the scintillation source and the PMT by mechanical means. This method proved inadequate in that the total variation was insufficient and the minimum output was not adequate.

At first, consideration was given to reducing the output by shielding the 5 ucurie radioactive source. This approach was not taken since a 0.5 ucurie source was available in the same size package as the original source for the same cost. The mechanical vernier was discarded in favor of control by variation of the high voltage similar to the means used for the

LED PMT, i.e., switched series resistances.

The output of the noise source was modified so that either polarity signal is available. This modification involved the use of an inverting amplifier at the summation mode of the outputs of the two PMT's.

Provision was made for external modulation of the LED. This involved the addition of an internal amplifier similar to the one used at the output of the internal square wave oscillator. The basic details of these modifications are indicated in Figure 2.1.

III. Noise Reduction Circuitry

3.0 Introduction

A technique for gamma pulse noise suppression by cancellation was introduced in the report mentioned earlier in Section II. This approach involves isolation of the gamma pulse from the signal, synthesizing a mirror image pulse and finally summing the original signal with the mirror image pulse to obtain a noise free signal.

3.1 Synthesizing the Gamma Mirror Image Pulse

The basic approach of this technique is to differentiate the original signal containing the gamma pulse and thereby remove the signal. The resultant differentiated signal is then integrated to obtain the original pulse reversed in phase by 180°.

This approach is shown in Figure 3.1. The output from the buffer amplifier is differentiated at the input to the inverting input of the 531 operational amplifier. Positive going signals at the output gate diode D_1 on during the integration time. Diode D_2 suppresses negative going swings at the output.

Difficulty was encountered with this circuit which was related to compensating the 531 operational amplifier. Normally a single capacitance is used between the output and the compensation node. It was found necessary to split the compensation as indicated in Figure 3.1.

The output of the differentiator-integrator is buffered from the summing amplifier by a variable gain noninverting amplifier stage using a 531 operational amplifier.

3.2 Delay and Summing

In the breadboard version it became apparent that it was necessary to delay the original signal prior to summing it and the image pulse. The delay required was of the order of 0.5 usec. As indicated in Figure 3.1 this delay is inserted between the signal post amplifier and the summing amplifier.

The delay circuit is an MFD filter designed to have a variable zero frequency delay τ_o. This circuit is a third order Thompson filter of the form described in the report mentioned in Section II; however, 531 amplifiers were used rather than 741's. Variation in τ_o was accomplised in discrete steps. It was decided to make τ_o variable in order to compensate for variations that might arise from wiring and component placement of the prototype instrument.

An MFM filter was used between the output of the summing amplifier and the final output of the instrument. The bandwidth of this filter was variable between 5KHz, 10KHz and 15KHz in three discrete steps. The circuit topology of this Butterworth filter is the same as the MFD Thompson filter with the desired characteristics obtained by appropriate matching of the

coefficients of the transfer functions. Addition of this filter makes it possible to evaluate either noise output or harmonic content of the signal for which the anticipated fundamental was about 4KHz.

3.3 Summary

In the breadboard version of this circuitry it was found possible to achieve 25 db suppression of the undesirable gamma pulses. These results were obtained using the Optical Signal and Random Noise Source Model II. A somewhat smaller value of suppression was obtained with the final prototype. Evaluation of the final circuitry indicated that the final form of the circuit layout had introduced additional delay, more than had been anticipated, such that optimum suppression was not possible. The suppression obtainable with this prototype was about 20 db.

3.4 Conclusions

Evaluation of the gamma noise suppression circuitry suggests two avenues that should be investigated to improve the efficiency of the prototype instrument. One of these is to improve the control of the delay in its early location in the circuitry by improved physical layout, and or choice of improved IC active devices. An alternative approach which should be investigated is the optimum location of the actual delay circuitry. THat is, it may be feasible to place the delay in the circuit prior to differentiation and thereby obtain more flexibility.

IV. IR Detector Scanning System

4.0 Introduction

This report covers the design and fabrication of the electronic instrumentation required for a solid state multiple detector and CCD readout

optical system. The detector scanning system consists of two packages, the Infra Red Detector Scanning System, IRDSS Model I, and the IR Det. 1A Aux. Unit. The IRDSS Model I is a clocked three phase MOS-FET gated system capable of supplying five output signals in a prescribed sequential format. The IR Det. IA Aux. Unit consists of a digital word generator for electronic evaluation of the CCD shift registers, a voltage monitor with eight variable bias supplies and a reset pulse required for correct operation of the output of the CCD units.

4.1 Basic Requirements

The IR detectors, Schottky diodes, are momentarily charged in parallel while isolated from their individual CCD input wells. This charge voltage pulse will be referred to as Setting Pulse or S. The detectors then are illuminated while completely isolated. After this "staring time", referred to subsequently as integration time, the signal from each detector must be transferred to the input of a three well CCD unit, one unit for each detector. After signal transfer each detector must be isolated from the charging circuit and the input CCD well during the serial readout of the CCD shift register and prior to the subsequent charge interval. This control circuitry will be described later in Section 4.4 concerned with Sequence Control.

The physical structure of the CCD units under consideration required three phase operation in conjunction with a master clock. The master clock was to be free running at a nominal frequency of 1 MHz with the PRF and Duty Cycle relatively independent of each other. Synchronization of the master clock with the three phase gate signals was not required by virtue of the synchronization afforded by the sequential control circuitry, as

will be seen in later sections.

The physical structure of the CCD units also required that the three phase gate voltages overlap. This requirement was met with what will be referred to as gate expander or pulse stretcher circuits.

Thus, the five output signals referred to for the IRDSS Model I, are the Setting Gate signal, referred to as S or its complement $\overline{S}$, the Synchronized Transfer Pulse, STP or its complement $\overline{STP}$, and the three stretched phase pulses referred to as $\phi_1(s)$, $\phi_2(s)$ and $\phi_3(s)$. All five of these gate voltages were to be variable between 0 and 20 volts. Isolation of the detectors also required that the S and STP gates have the capability of negative off-set bias.

The reset gate voltage of the IR det. IA Aux. Unit did not require an offset bias, but otherwise must meet the same requirements of the three phase gate voltages. The digital word generator output was set at 0 to 3 volts with an offset adjustable from 0 to 4 volts.

One final requirement was that the electronic system was to be flexible, with adequate test points and capable of being modified readily. A block diagram of the overall system is given in Figure 4.2.

4.2 Organization

In the interest of flexibility the physical system for the IRDSS Model I consists of five plug-in modules in a standard rack-mounting cage. The five modules are numbered and labelled as follows:

Panel 1	Master Clock
Panel 2	Sequence Control
Panel 3	Clock-Gate, Three Phase Generator

Panel 4 Gate Expander - Gate Driver

Panel 5 Power

The IR Det. IA Aux. Unit consists of three plug-in modules numbered and labelled as follows:

Panel 6 Digital Word Generator

Panel 7 Voltage Monitor

Panel 8 Bias Control

Details of the circuits for these panels will be discussed in subsequent sections. Both of these units are shown in Figure 4.1.

4.3 Master Clock - Panel 1

The Master Clock circuit is an astable multivibrator circuit composed of two monostable IC's, SN74123, feeding back on one another. See Figure 4.3 The output pulse width of each of the monostable circuits is determined by a single RC combination. For this application a variable resistance, common to both units, in conjunction with individual C's, controls the duty cycle. A second variable resistance in series with V_{CC} and the duty cycle variable resistance controls the frequency or PRF. Interaction between these two variables was relatively insignificant.

The desired output from the Master Clock, Q or $\overline{Q}$, may be selected by a switch located on the front panel. Isolated clock pulses for the pulse stretcher circuits and the clock gating circuitry were made available by means of two inverters of the hex inverter SN7404.

4.4 Sequence Control - Panel 2

The Sequence Control circuitry consists of three monostable multivibrators in cascade using two SN74123's as indicated in Figure 4.4. In

the subsequent discussion these monostable units will be referred to as FF_1, FF_2 and FF_3. FF_1 generates the S and $\overline{S}$ time interval. The $\overline{S}$ output is the input to the second monostable circuit, FF_2. "Staring time", or integration time is determined by FF_2 and its associated timeconstant. FF_3 is triggered by the output of FF_2 and generates the Initial Transfer Pulse, ITP.

Provisions have been made for three possible inputs to the Sequence Control Circuitry. A front panel switch selects these as EXT, FTP or INT. The input EXT is a special input for a synchronizing signal from a light shutter. Such a signal is processed internally by two operational amplifiers which provide for both phase and magnitude control of the input synchronizing signal.

The FTP input is also an external input; however, it provides a means of synchronization by means of any signal source having the capability of triggering FF_1.

The INT input synchronizes the Sequence Control Circuitry by means of an internal astable multivibrator circuit utilizing an NE555 timer. Supply voltage for the NE555 circuit is removed on the other two input switch positions to avoid interaction. The PRF of the NE555 circuitry is controllable from the front panel with the INT PRF control. The pulse width is fixed at 1 millisecond and the PRF is variable from 10 to 100 Hz. See Figure 4.13 for waveforms available at Panel 2.

4.5 Clock Gate, Three Phase Generator - Panel 3

A working diagram of the Clock Gate and Three Phase Generator circuitry is shown in Figure 4.5. The Clock Gate circuitry consists of a dual D type

flip-flop, SN7474, and AND gate, a Delay consisting of four buffer amplifiers in cascade, four units of an SN7407 Hex Buffer, and an output OR gate. The Three Phase Generator circuit consists of a dual JK Master-Slave Flip-Flop, SN7473, and a NOR gate, one gate of the SN7432 Quad Nor Gate.

Prior to an input ITP to the D_1 flip-flop there is no output from either D type flip-flops or the Delay. Consequently, the output from the OR gate to the Three Phase Generator is the Master Clock signal, and the CK signals for each JK unit is synchronized with the Master Clock. This applies as long as the ITP signal is low, or there is no output from the Delay into the OR gate.

Operation of the Three Phase Generator can be explained by means of the JK truth table and the interconnections of the two JK flip-flops. Note in Figure 4.5 that J_1 and Q_2 are common and Q_1 and J_2 are common. $K_1 = K_2 =$ 5 volts, or both are maintained at a logic level of 1. This means that only the bottom two conditions of the truth table in Figure 4.6 apply to the Three Phase generator circuit.

JK flip-flops operate only on the *fall* of the CK signal. Thus, from the truth table if J = K = 1 prior to the fall of the CK signal, then after the fall of the CK signal the output of the JK flip-flop will be inverted from its level prior to the CK signal. If J = 0 and K = 1 prior to the fall of the CK signal, then the output goes to 0 after the fall of the next CK signal.

Using the truth table of Figure 4.6 one can construct a table of logic levels for J_1, Q_1, etc. which will demonstrate the generation of two of the three phase pulses, ϕ_2 and ϕ_3. This program is shown below and starts

at line one with the CK high and the *assumed* initial logic levels. Each fall of the clock is shown as ↓ and each succeeding line gives the logic levels after the fall of the clock.

Three Phase Generator Program

	J_1	K_1	Q_1 (ϕ_2)	J_2	K_2 (ϕ_3)	Q_2	$\overline{Q}_2$	CK
Logic levels prior to first fall of CK	1	1	0	0	1	0	1	
	1	1	1	1	1	0	1	↓1
	0	1	0	0	1	1	0	↓2
	1	1	0	0	1	0	1	↓3
	1	1	1	1	1	0	1	↓4
	0	1	0	0	1	1	0	↓5

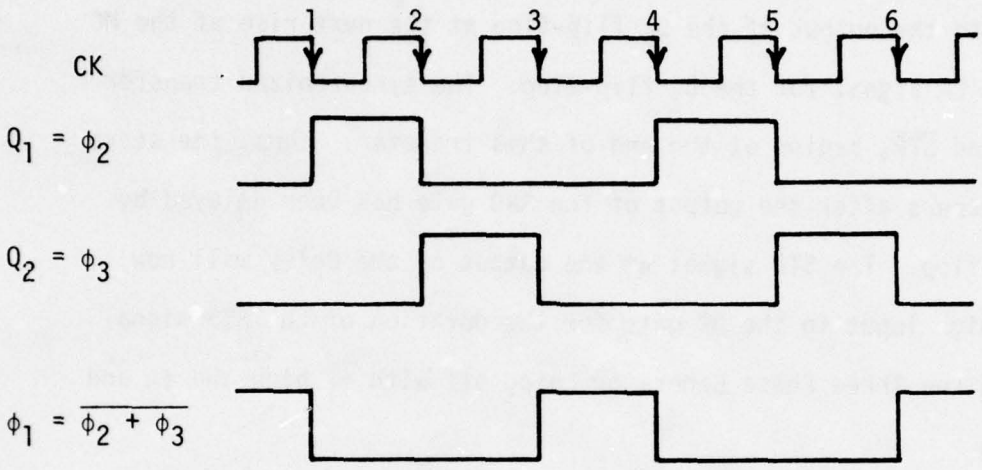
After the first fall of CK, Q_1 has gone to the 1 level with Q_2 unchanged, or still at the 0 level. After the second fall of CK, Q_1 is at the 0 level and Q_2 has gone to the 1 level. After the third fall of CK both Q_1 and Q_2 are at the 0 level. Since $Q_1 = \phi_2$ and $Q_2 = \phi_3$, it can be seen that starting from the given assumptions ϕ_2 and ϕ_3 have been generated at the desired interval and phase.

Φ_1 is generated at the output of the NOR gate. The NOR gate will go to the 1 level only when both inputs are at the o level. Otherwise the output remains at the 0 level, or, if at the 1 level, returns to the 0 level if either input is at the 1 level.

Note that after the third fall of CK both inputs to the NOR gate are low giving a high output. After the fourth fall of CK, Q_1 goes to a 1 level with Q_2 remaining at the 0 level and the output of the NOR gate returns to

the 0 level. Thus, during the third and fourth fall of CK, during the interval when ϕ_2 and ϕ_3 are both at a 0 level, ϕ_1 is generated.

These results are demonstrated in a timing diagram shown below.



Timing diagram for Three Phase Generator

This discussion is valid only as long as there is only the MC signal at the input to the OR gate of the Clock Gate circuit. If a constant level of 1 is maintained at either input of the OR gate, the Three Phase Generator will be inoperative. Thus, it is possible for the Three Phase Generator to be turned off for the duration of the STP signal at the output of the Delay circuit. This capability is necessary since during the transfer of data to the CCD array, the synchronized transfer time, CCD readout should not occur.

Now assume that the Sequence Control circuitry initiates the FTP signal at the D input to the D_1 flip-flop and one input of the AND gate. The other input of the AND gate Q_1 of the D_1 flip-flop. The D_1 input is transferred to Q_1 only on the next rise of $\overline{\phi}_3$, the CK signal for the D_1 flip-flop. Thus, the output from the AND gate will be delayed for the

interval between the initiation of the input ITP and the next rise of $\overline{\phi_3}$ and ϕ_1.

The AND gate going high at the D input of the D_2 flip-flop will be transferred to the output of the D_2 flip-flop at the next rise of the MC which is the CK signal for the D_2 flip-flop. The synchronized transfer pulse, STP and $\overline{\text{STP}}$, begins at the end of this transfer. Thus, the start of the STP occurs after the output of the AND gate has been delayed by the D_2 flip-flop. The STP signal at the output of the Delay will now maintain a high input to the OR gate for the duration of the STP signal resulting in the Three Phase Generator being off with ϕ_1 high and ϕ_2 and ϕ_3 being low.

At the end of the ITP signal the AND gate terminates the D signal of the D_2 flip-flop immediately. On the next rise of the MC the 0 level of the D input is transferred to the output of the D_2 flip-flop terminating the STP and $\overline{\text{STP}}$ signals. The STP signal at the output of the Delay is terminated after a short delay determined by the characteristics of four buffer amplifiers in cascade. At the next fall of the MC the Three Phase Generator is again operative.

The Delay circuit is not crucial. It insures that the output of the OR gate does not go to zero at the end of the STP while the MC signal is low. It does not affect the operation at the beginning of the STP since ϕ_1 is already high, or at the 1 level.

A scope synch signal is available as the output of a unity gain operational amplifier. The amplitude is variable and may be referenced to either STP or $\overline{\text{STP}}$. The digital word sync signal is also available on this panel.

4.6 Gate Expander, Gate Drivers - Panel 4

An explanation of the Gate Expander, pulse stretching or overlap circuitry, will make use of the diagram of Figure 4.7. The delay properties of D type flip-flops is used to extend the width of each phase pulse by the down time of a single cycle of the MC.

In Figure 4.7 the ϕ_1 pulse is the input signal to the D_1 input and one input of the NOR gate. The other input to the NOR gate is Q_1 of the D_1 flip-flop.

The D_1 level is transferred to Q_1 only on the rise of the CK signal which in this case is the MC. The output of the NOR gate is low for any combination of inputs other than both being low. Both inputs will be low during the pulse interval that ϕ_1 is low, and the NOR gate output will be high.

Now consider that ϕ_1 rises. The output of the NOR gate drops beginning $\overline{\phi}_1(s)$. On the next rise of the MC, Q_1 will go high and remain high until the next rise of the MC occurs with D_1 low. D_1 goes low at the end of the ϕ_1 pulse, but Q_1 does not drop until the next rise of the MC. When this occurs both inputs of the NOR gate are low and the $\overline{\phi}_1(s)$ output is terminated, i.e. the output of the NOR gate goes from low to high. Thus, the $\overline{\phi}_1(s)$ pulse is a negative going pulse having a width of the original ϕ_1 pulse plus the down time of one cycle of the MC.

$\overline{\phi}_2(s)$ and $\overline{\phi}_3(s)$ are obtained in the same manner. Inversion by the phase driver amplifiers gives the proper phase for the CCD gates. Waveforms for $\phi_1(s)$, $\phi_2(s)$ and $\phi_3(s)$ are shown in Figure 4.14.

Commercially available IC Clock Driver amplifiers, MH0026C, are used for the three phase pulses. The MH0026C is a dual amplifier with a common supply voltage input. Since three drivers are required two units are used resulting in one of the four amplifiers not being used.

Amplitude of the three phase outputs is controlled simultaneously by means of an active voltage source. This circuit is an emitter follower configuration which reduces the +30 volts to 0 - 20 volts by a single potentiometer. This control is on the front panel labelled PHASE LEVEL.

Initial off-set of each of the phase outputs is individually controlled by independent auxiliary biasing sources. These controls are referred to on the front panel as PHASE ADJUST.

The S and T output driver amplifiers are shown in Figure 4.8. The two amplifiers are identical and use an NPN and a PNP BJT in a noninverting complementary configuration. Both type BJT's come four to a DIP package. The package diagram for each type device is shown in Figure 4.8. The terminal designations on the schematic correspond to the DIP package numbering.

4.7 Power Supply - Panel 5

Details of the supply voltage circuitry are shown in Figure 4.9. Input power requirements are nominally 115 volts at 60 Hz for each of the three self contained d-c supplies.

The dual supply is rated at 5 volts at 500 ma and ±15 volts at 60 ma. The 30 volt supply is rated at 200 ma. The single 5 volt supply, used for the DVM, is rated at 1 ampere.

Five LED's are used as panel indicators for the five d-c voltages. The 5 volt 1 ampere supply fuse is located behind the panel. The other two supplies have separate fuses located on the front panel.

4.8 IR DET IA AUX Unit

This auxiliary unit consists of three plug-in modules designated as panels 6, 7 and 8. Panel 6 contains a digital word generator for testing the CCD shift registers with an electronic signal input. Panel 7 is a DVM voltage monitoring circuit that also contains a reset pulse driver amplifier. The output of this amplifier replaces the charge lost by the source follower used for the output stage of the CCD shift register. Panel 8 is a variable bias supply used for controlling the voltage levels at eight different points in the CCD control circuitry.

4.9 Digital Word Generator - Panel 6

The digital word generator output is a series of pulses. The number of pulses determines the word length which is controlled by the Word Length switch on the front panel. This switch is labelled 2^0 through 2^5 for word lengths corresponding to 1, 2, 4, 8, 16 and 32 pulses respectively.

The time interval between the start of one word and the initiation of the next word is referred to as the word period. This interval is specified in terms of the number of pulses that could occur for a particular word period. The Word Period switch on the front panel is labelled 2^6 through 2^{11} for word periods of 64, 128, 256, 512, 1024 and 2048 pulses respectively.

The Word Period and the Word Length controls are independent of each other. As an example, let the Word Length switch be set to 2^3 and the

Word Period switch be set to 2^7. The output of the word generator would be 8 pulses followed by no pulses for an interval corresponding to 120 additional pulse intervals. See Figure 4.15 which is a photograph of the output of the word generator for a 4 bit word.

A working diagram of the Word Generator circuit is shown in Figure 4.10. The output pulses from gate A_3 are generated by two monostable flip-flops, SN74123, connected in cascade. The first flip-flop output, the input to the second flip-flop, is delayed by the variable RC time constant labelled DELAY on the front panel. The final output pulse width is controlled by the variable RC time constant of the second flip-flop labelled on the front panel as WIDTH.

The final output of the word generator has a controlled off-set as well as a variable amplitude. The off-set is adjustable from 0 to 4 volts by means of the front panel control called BIAS. The amplitude of the output word is variable from 0 to 3 volts by means of the front panel control called LEVEL.

Input pulses to the first monostable flip-flop are controlled by a two input NAND gate. One input to this NAND gate, A_2, is a constant pulse train having the frequency of either the internal Master Clock or an external Clock signal. The other input to the control NAND gate is the Q output of a D-type flip-flop, SN7474. An input to the first monostable flip-flop is determined by the proper coincidence of the two inputs to the controlled NAND gate, A_2.

The logic level of the Q output of the D-type flip-flop is controlled by the Clear and Preset levels. When the Clear input goes low, or to a 0

logic level, the Q level will go to a 0 logic level. When the Preset input goes low the Q output level will go high, or a 1 logic level.

The Clear signal is controlled by the outputs of a ripple counter. As indicated in Figure 4.10 the ripple counter consists of 12 four-bit binary counters connected in cascade, (SN7493). The input to the first counter is the same constant pulse train used as one input to A_2. The outputs of the first six counters correspond to the Word Length switch positions 2^0 through 2^5. The Preset signal is controlled by the outputs of the last six counters by means of the Word Period switch positions 2^6 through 2^{11}.

The Reset inputs to all counters are tied together with a common connection to the pole of the Word Period switch and one input to the NAND gate A_4 which controls the Preset signal. When the Reset signal goes high all counters are reset to a 0 output logic level and the Preset signal, the output of A_4, also goes low resulting in Q of the D-type flip-flop going high.

Assume that at time t_0 all counters have been reset to a 0 logic level, the Word Length switch set to 2^3 and the Word Period switch set to 2^6. Resetting the counters to a 0 logic level has left Q of the D-type flip-flop in the high state. The A_2 gate will now trigger the first monostable flip-flop and the word generator output will be a pulse for the first 8 inputs to the counter. The 8th input will result in the output of the 4th counter going high. The Clear signal at the output of the NAND gate B_1 will go low. This will put the Q output of the D-type flip-flop at a low level and deactivate the A_2 NAND gate, thereby giving no further output from the word generator. On the 64th input to the first counter the output of the 7th counter will go

high. All counters are reset to a 0 level, Preset goes low, Q output goes high and the sequence begins anew.

4.10 DVM Monitor and Reset Pulse - Panel 7

The input to the DVM may be connected directly to the EXT VOLT jacks on the front panel - VOLTAGE SELECTOR switch set to EXT - or switched to 10 hard wired monitor points. The actual DVM input can only take positive voltages not exceeding +1.99 volts. An internal attenuator is used to rescale the meter indication to +19.9 volts full scale.

Two of the hard wired monitor points are negative voltages. Inverting circuitry is used at each of these points so that the actual monitored voltage is positive as required by the DVM. On the front panel on either side of the DVM is an LED. On the left side the LED is marked -. On the right side the LED is marked +. These LED's indicate the actual polarity of the original monitored voltage.

The setting of the VOLTAGE SELECTOR switch is indicated by an LED located adjacent to the control knob for each of the 10 hard wired monitor points. Eight of these are located on Panel 8, one on Panel 7 and one on Panel 4 of the IRDSS.

Circuit details of the DVM monitor panel are shown in Figure 4.11. Figure 4.11 also indicates the circuit details of the reset pulse amplifier. The driver amplifier is the same as that used for the three phase drivers with the exception that no provision is made for an off-set voltage. The amplitude is variable from 0 to 20 volts.

As indicated in Figure 4.11 the pulse width of the reset pulse is determined by the coincidence of the inputs to a two input NAND gate. One of these inputs is ϕ_2 and the other ϕ_1'. Both of these inputs are obtained from the Pulse Stretcher and Gate Driving Amplifier module, or Panel 4. ϕ_1' is the Q output from the ϕ_1 D-type flip-flop. With these two signals the reset pulse width is equal to the amount that the original phase pulse is stretched, i.e., the difference between ϕ_1 and $\phi_1(s)$. See Figure 4.15a.

4.11 Bias Control - Panel 8

Circuit details of the bias control panel are shown in Figure 4.12. Five emitter followers provide voltage sources variable from 0 to 20 volts. One source provides 0 to 10 volts with a vernier control from 0 to 5 volts. One negative provides 0 to -5 volts and another 0 to -10 volts. The two negative sources are monitored by means of unity gain inverters as indicated in Figure 4.12.

4.12 Operation, Evaluation and Modifications

Waveforms at the output of the CCD detector chip for two modes of operation are shown in Figures 4.16 and 4.17. Figure 4.16 is the output using a four bit word input to the shift register. Figure 4.17a is the CCD output in the vidicon mode using a black body source at a temperature of 300°C wiht the chip temperature at 88°K. Figure 4.17b is for the same conditions with the detectors not illuminated.

In using this system for investigating the characteristics of a particular detector CCD shift register chip it became evident that certain modifications would enhance the possibility of improved operation of the chip. Improved sensitivity could be obtained by operating at a significantly

lower clock frequency than 200 KHz, reduced noise should be obtained by using a sample and hold circuit at the output of the CCD and some means of obtaining a fat zero for the CCD register should improve the transfer efficiency.

Operation at 9 KHz led to difficulties which were traced to the coupling capacitors and the off-set circuitry used between the output of the driver amplifiers and the phase gates. Experience indicated that the need for individual phase off-set control was an over specification. Consequently the coupling capacitors, shown in Figure 4.7, along with the off-set circuitry were eliminated and the phase gates were driven directly from the output driver amplifiers.

Reduction of noise, particularly phase voltage spikes, was accomplished by means of a sample-hold circuit, S-H, at the CCD output using the reset pulse on the chip as a reference. This circuitry is shown in Figure 4.18. The effectiveness of this circuitry is indicated in Figure 4.19. Figure 4.19a is an expanded portion of the flat region of the output of Figure 4.17a without the S-H circuit indicating the presence of the phase spikes. Figure 4.19b is the output using the S-H circuitry and the improvement is evident.

Improvement in the transfer efficiency was obtained by means of a "fat zero slosh" circuit, FZS, which was designed to provide a fat zero prior to the rise of ϕ_3. This circuitry is shown in Figure 4.20. An initial pulse is generated by ANDing $\phi_1(s)$ and $\phi_2(s)$. The inputs to the FZS are $\overline{\phi}_1(s)$ and $\overline{\phi}_2(s)$ which are inverted prior to the AND gate. This approach was taken because of the availability of $\overline{\phi}_1(s)$ and $\overline{\phi}_2(s)$ on Panel 4 of the IRDSS.

The output of the AND gate triggers MV1 which generates a pulse with a variable width of 25-104 useconds. Q_1 output is available at test point B_1. The $\overline{Q}_1$ output of MV1 triggers MV2 generating the FZS pulse at $\overline{Q}_2$ with a variable width of 10-40 useconds. (Q_2 output is available at test point B_2.) This pulse is amplified by a buffer amplifier with a variable output giving a negative pulse referenced to 15 volts, i.e., the FZS normally sits at 13.5 volts and may be driven almost to zero.

The output pulse at $\overline{Q}_1$ controls the location of the FZS. It can be located 25 useconds after the output of the AND gate of 104 useconds later or any other position between these two extremes. With the MC running at 9 KHz the FZS will always occur prior to the rise of ϕ_3.

Waveforms at the various points in the FZS circuit are shown in Figure 4-21. CCD output for vidicon mode of operation using both the S-H abd FZS circuitry are shown in Figure 4.22. These figures are for a black body temperature of 120°C and a chip temperature of 88°K.

4.13 Future Improvements

Evaluation of the IRDSS system to this point suggest that further improvements are possible without major changes in the existing modules. One improvement would be an extension of the staring time when using the vidicon mode of operation. The S-H module could be improved by a better basic S-H unit, and greater flexibility in the location of the control pulse as well as its variable width. A preamplifier at the CCD output could provide inceased sensitivity along with isolation and elimination of the d-c offset. Further reduction of noise may be possible by using additional filtering. This possibility will require an investigation to determine the appropriate type filters and their location in the overall system.

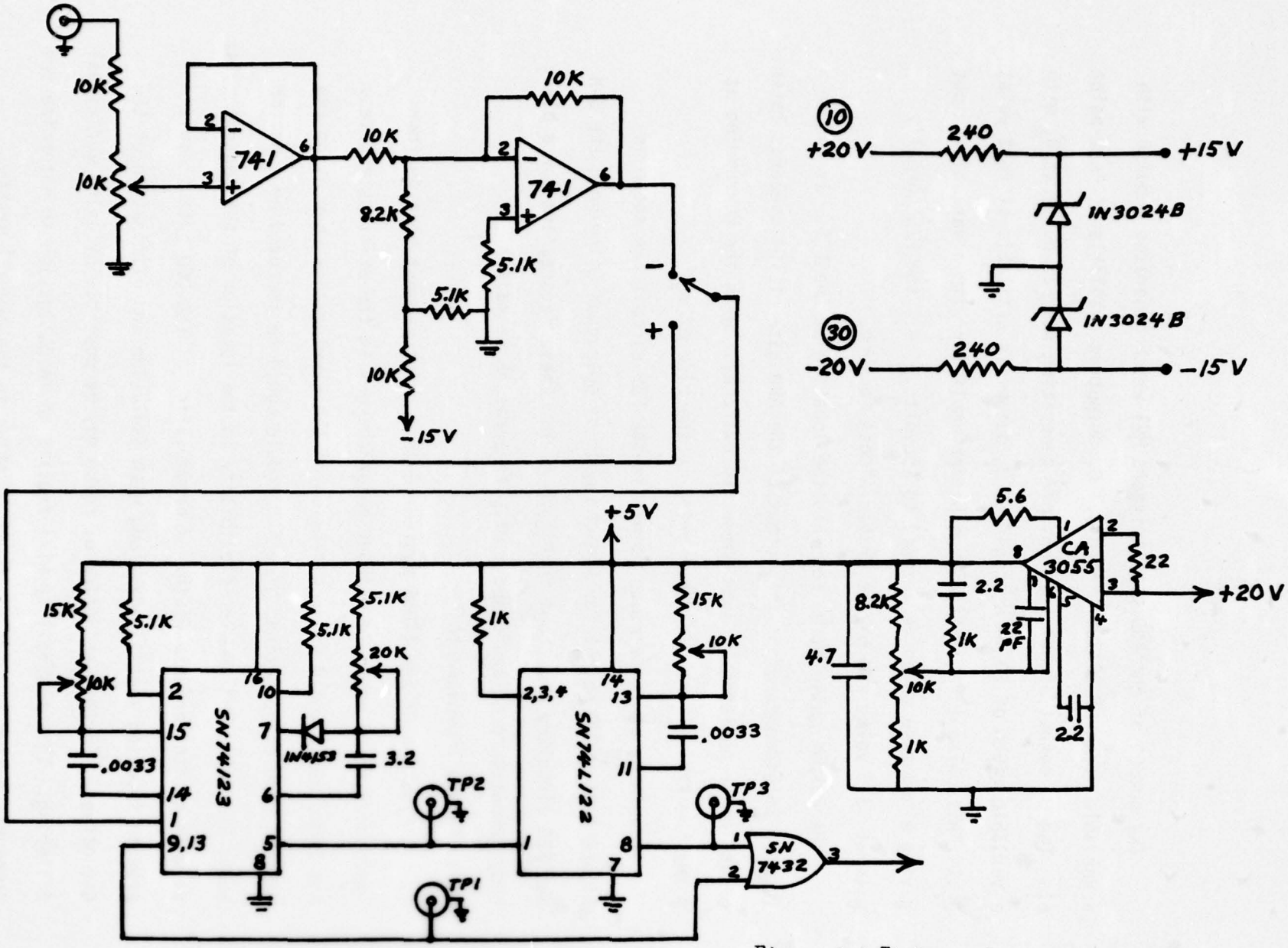


Figure 1.1 Timing and control circuitry

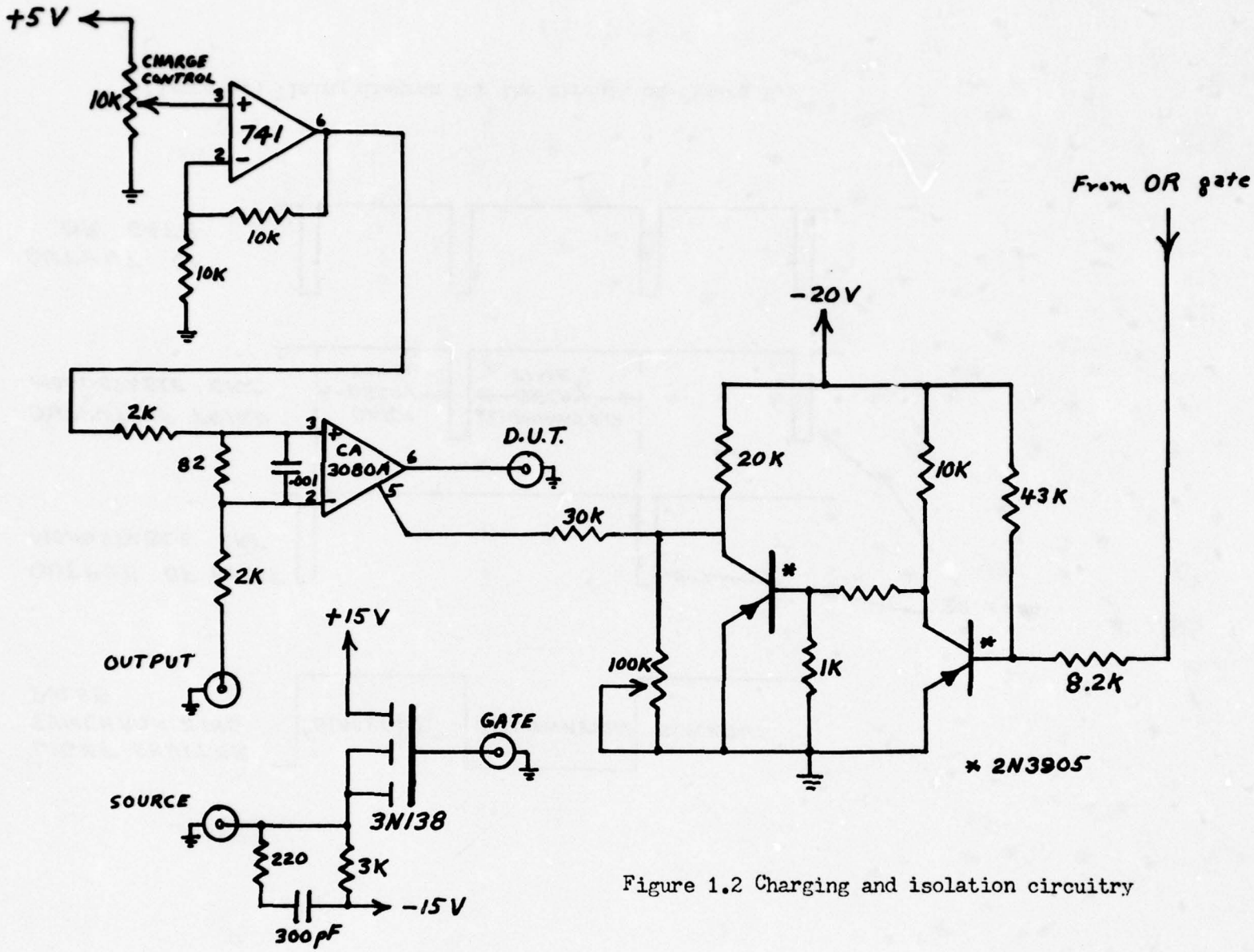


Figure 1.2 Charging and isolation circuitry

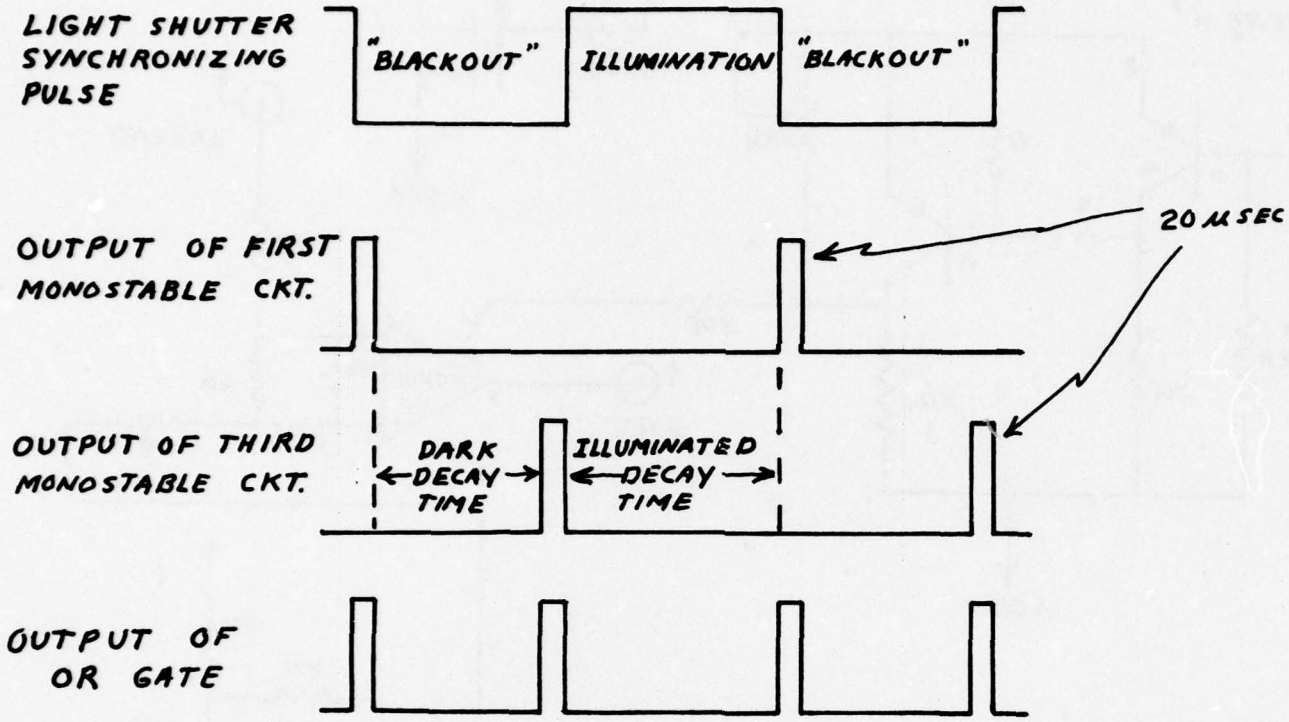


Figure 1.3 Timing diagram for the circuit of Figure 1.1

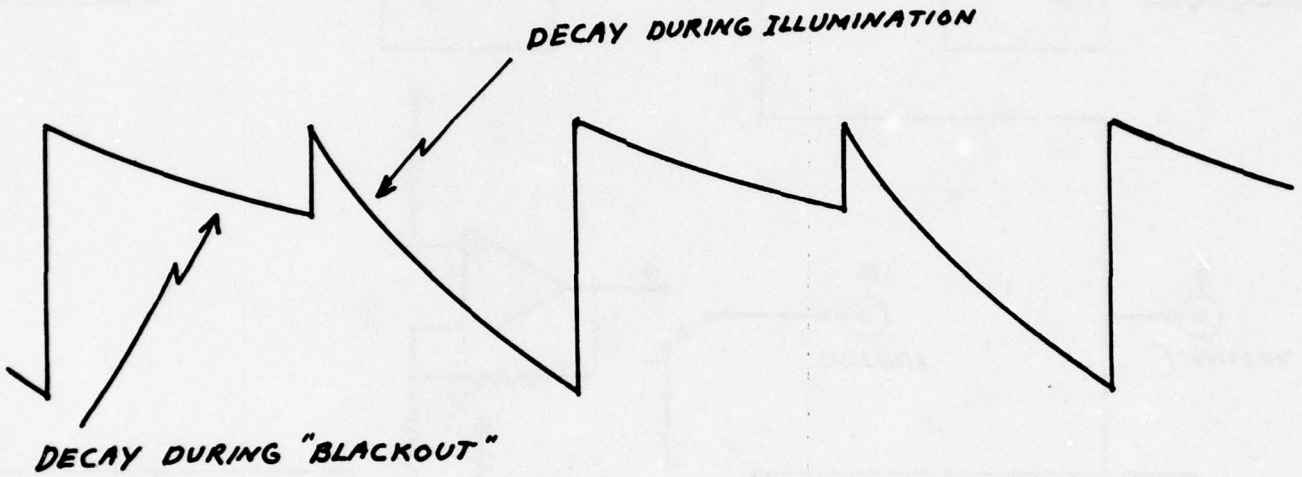


Figure 1.4 Discharge waveforms for a Schottky diode during "blackout" and while illuminated

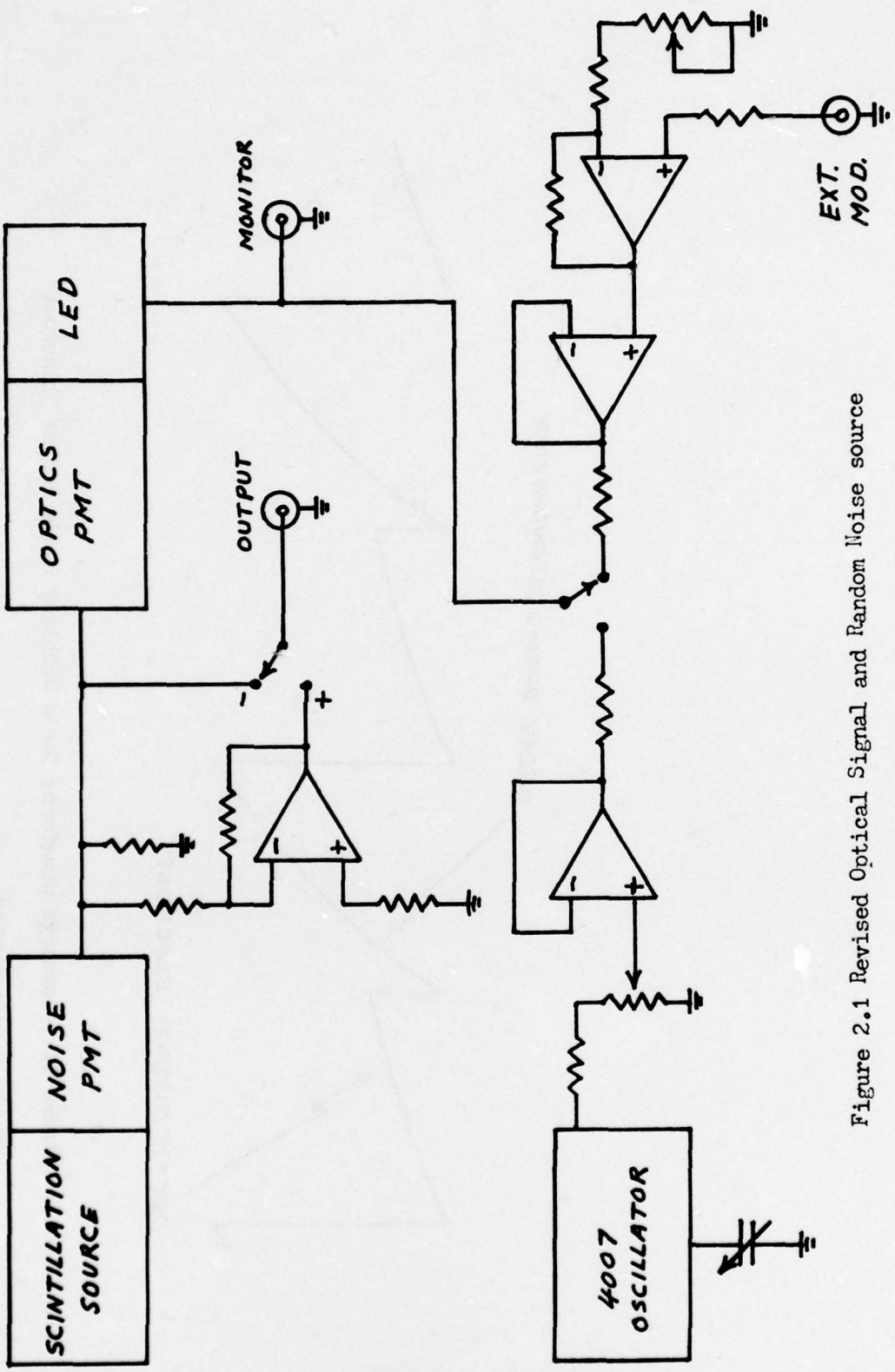


Figure 2.1 Revised Optical Signal and Random Noise source

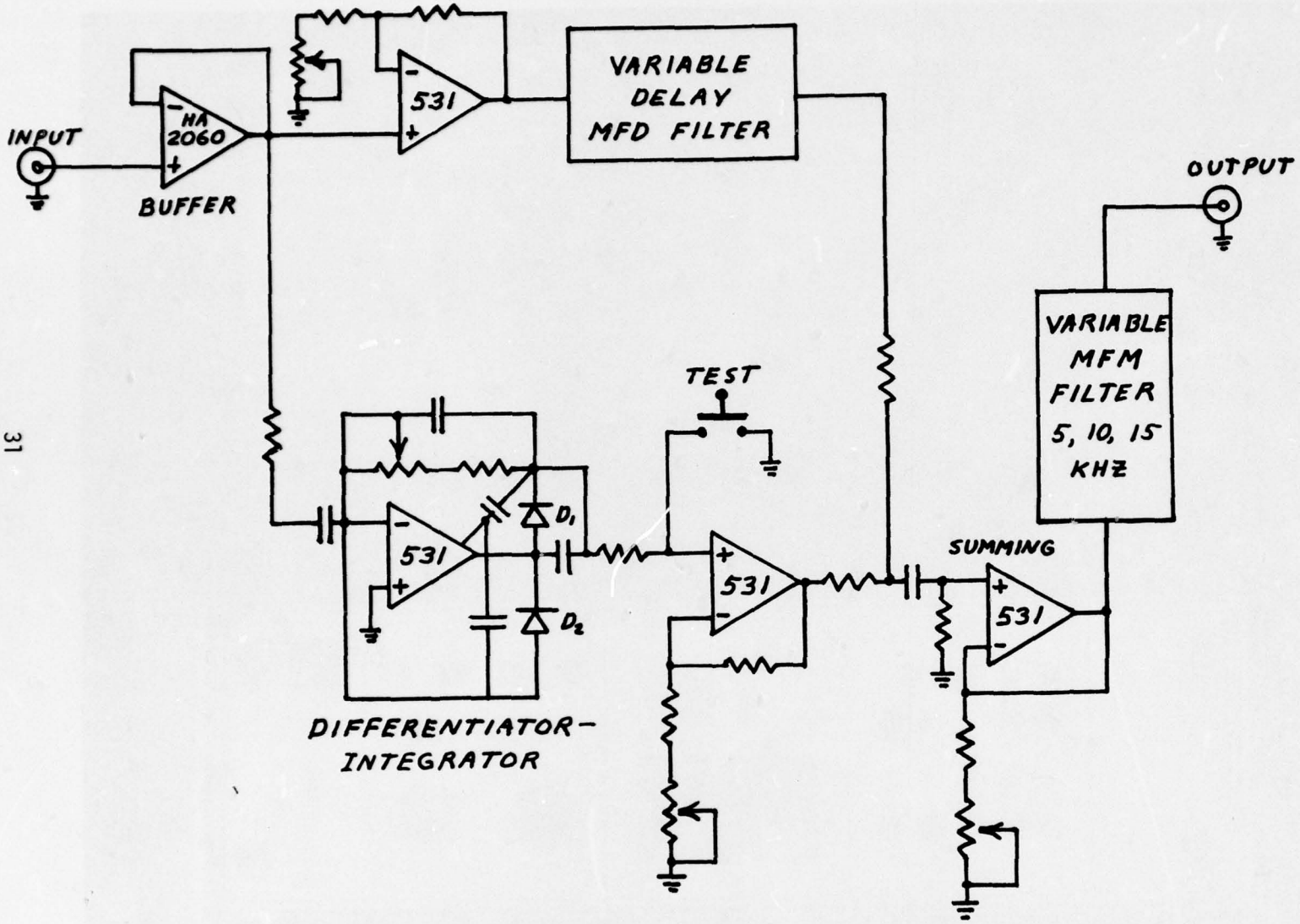


Figure 3.1 Noise cancellation circuitry

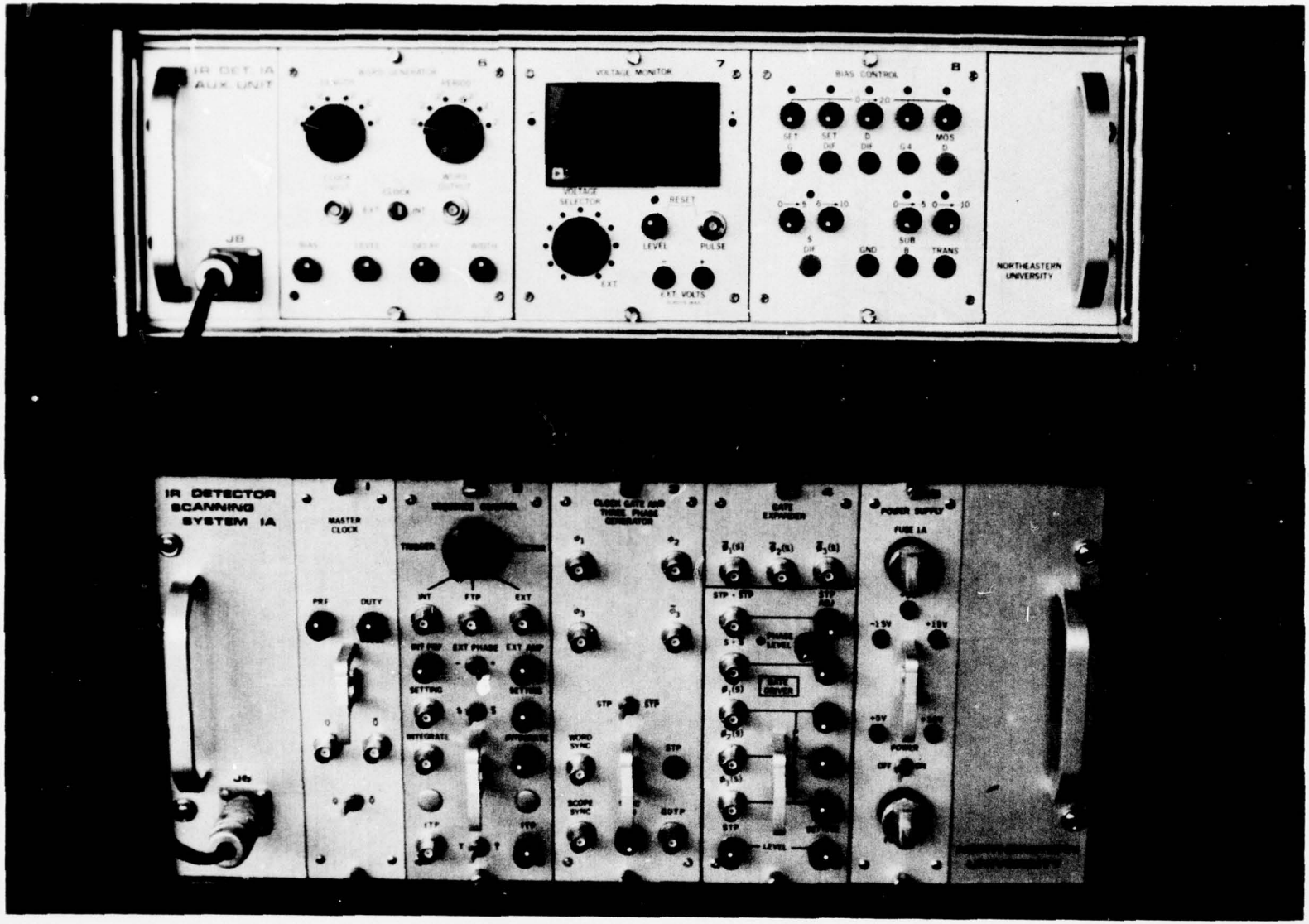


Figure 4.1 IRDSS Model I and IR Det IA Aux Units

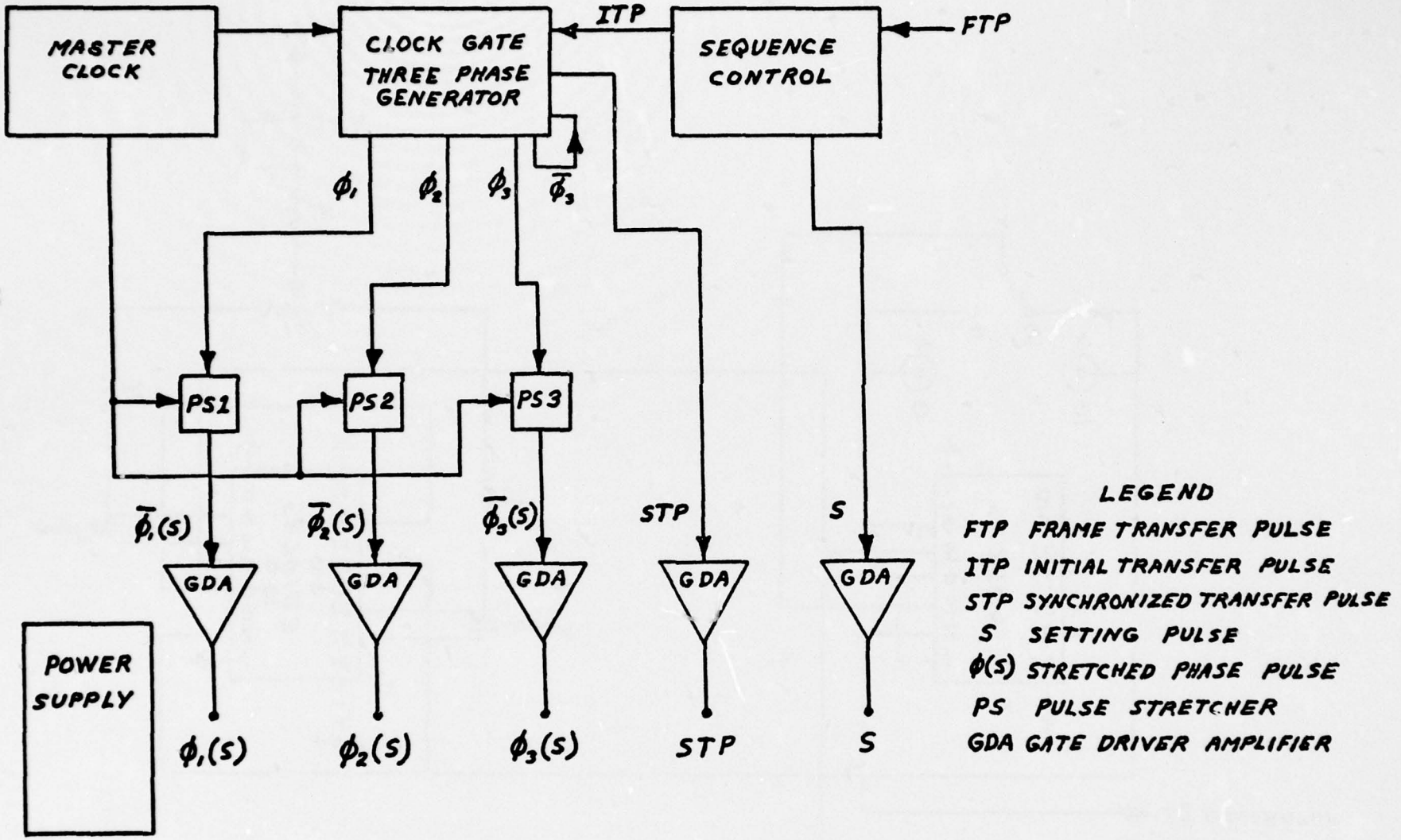


Figure 4.2 Block Diagram of IRDSS Model I

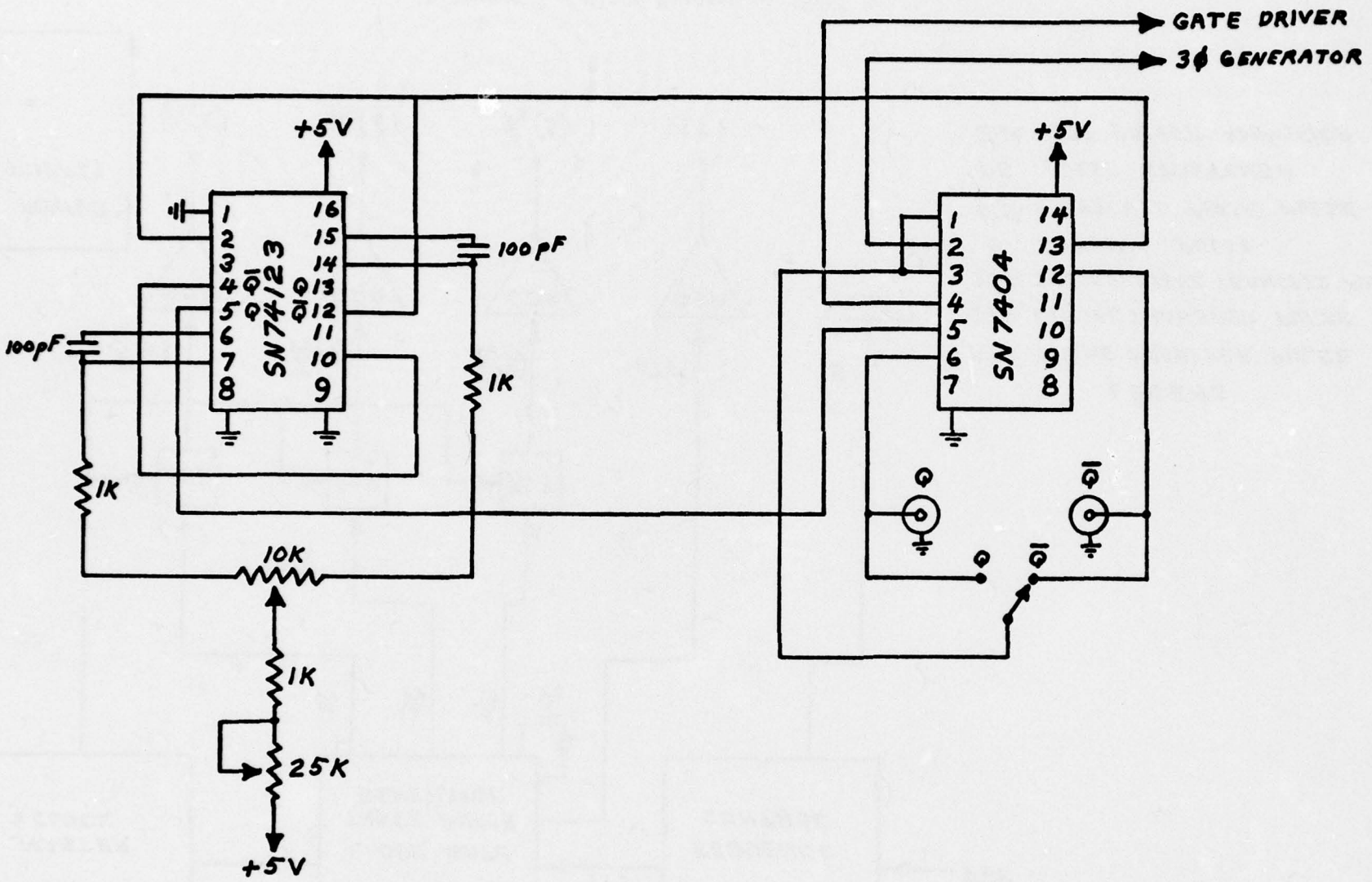


Figure 4.3 Master Clock Circuitry

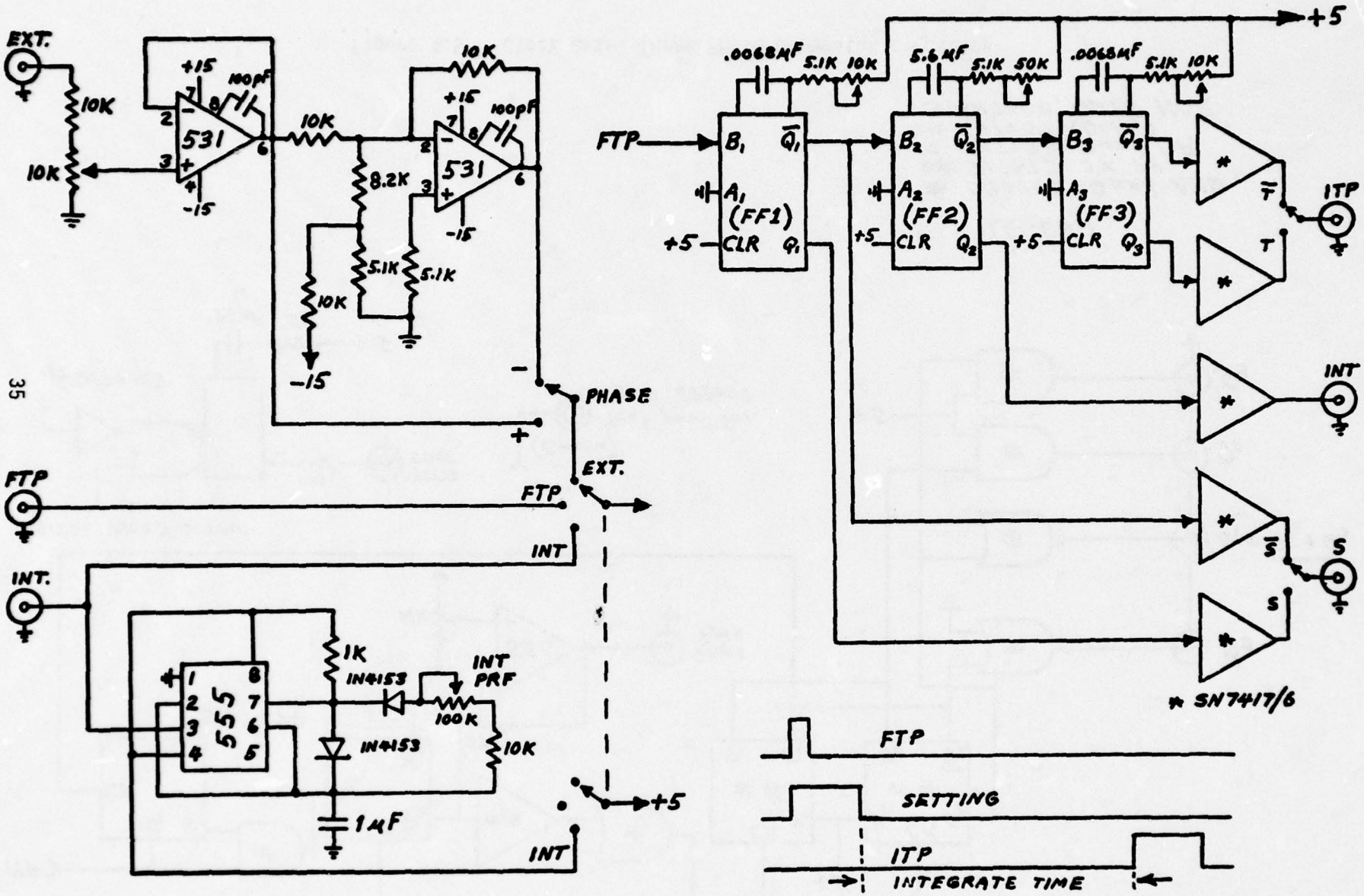


Figure 4.4 Sequence Control Circuitry

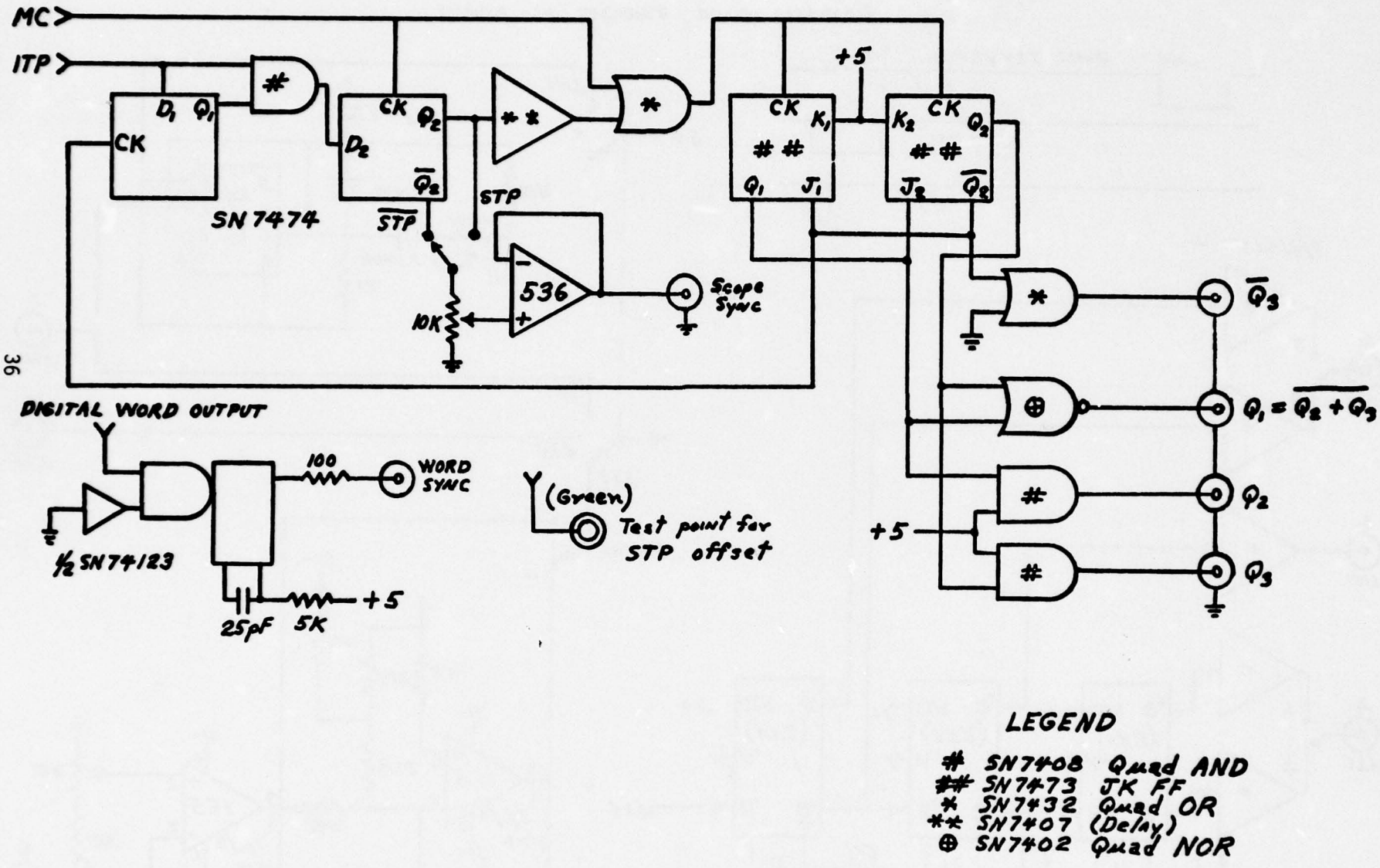
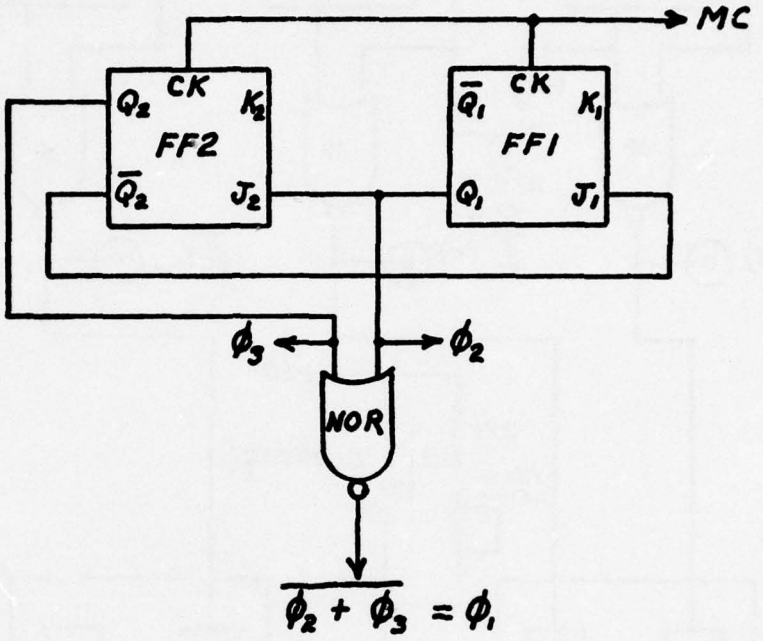


Figure 4.5 Clock Gate, Three Phase Generator circuitry

BASIC THREE PHASE GENERATOR



J-K
TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
1	0	1
0	1	0
1	1	$\bar{Q}_n$

Figure 4.6 Basic three phase generator and JK truth table.

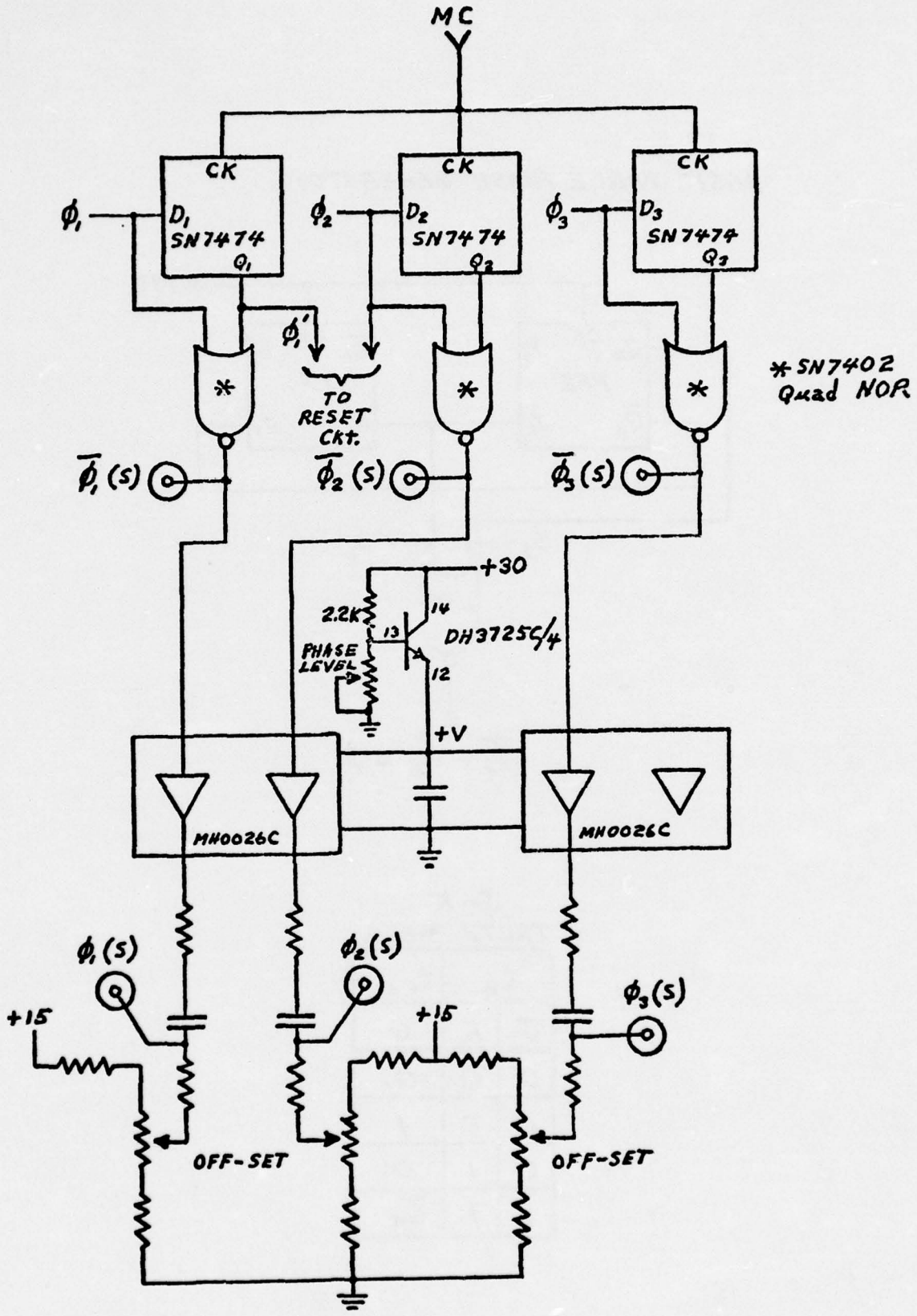
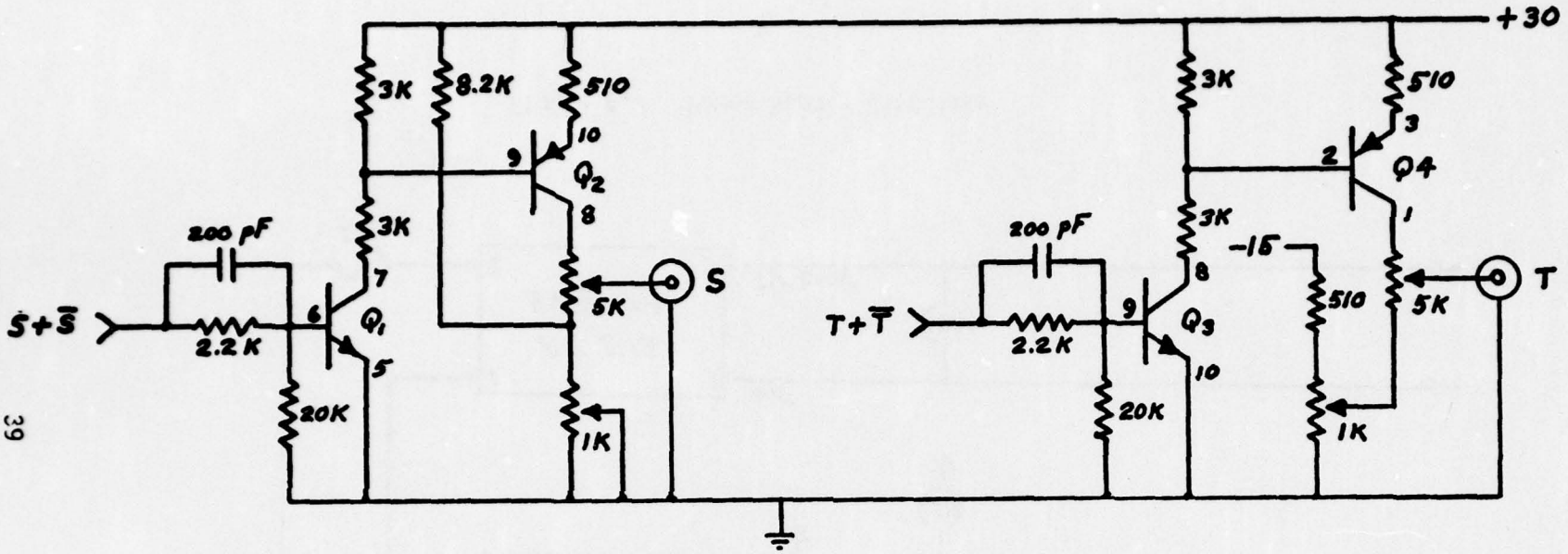


Figure 4.7 Gate Expander, Gate Driver Circuitry



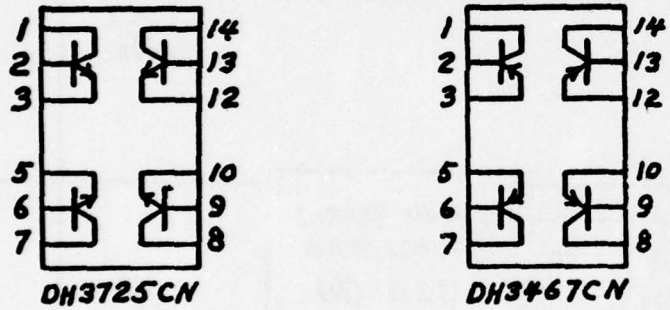


Figure 4.8 Setting and Transfer Driver Amplifiers

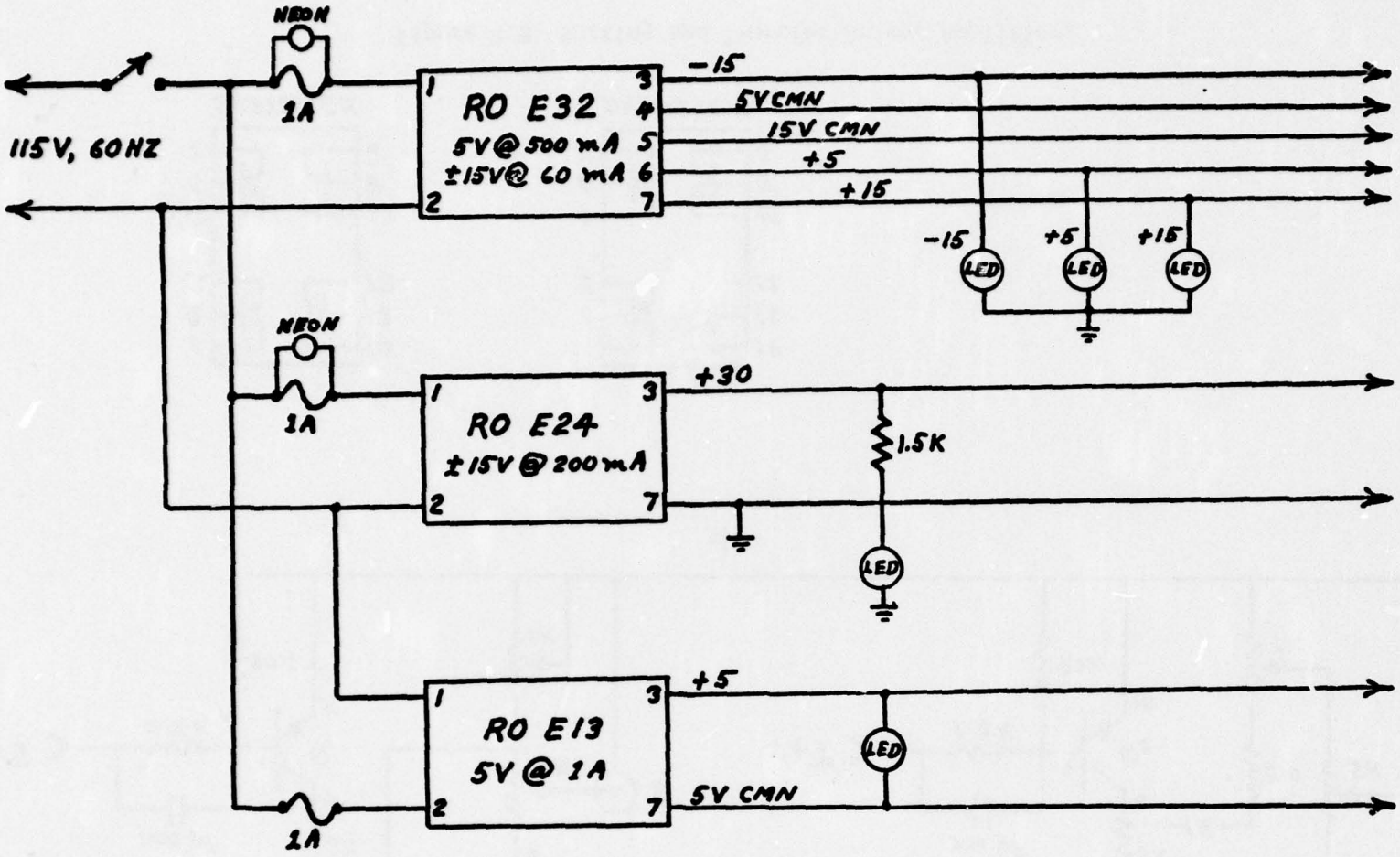


Figure 4.9 Power Supply Circuitry

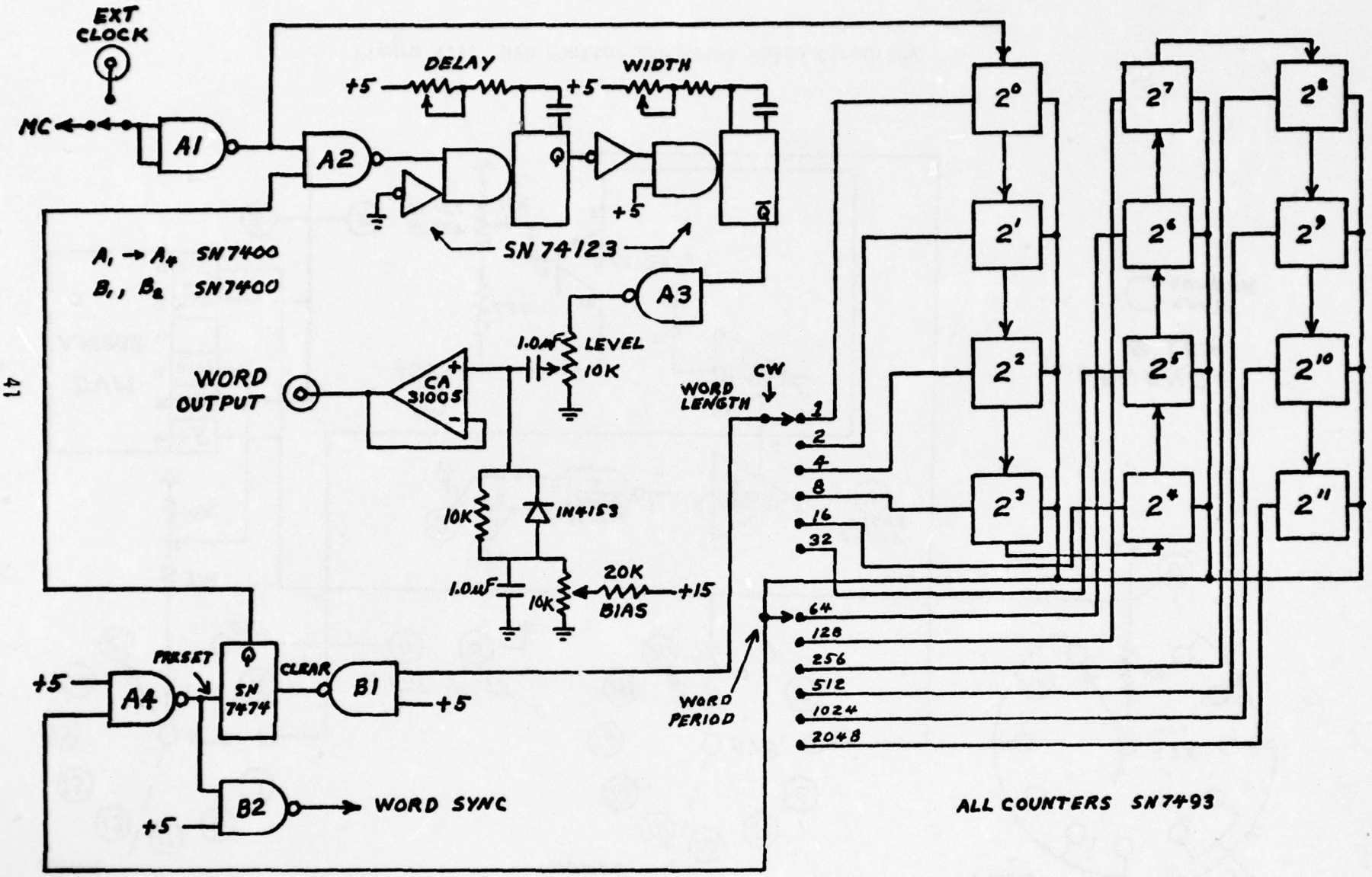


Figure 4.10 Digital Word Generator Circuitry

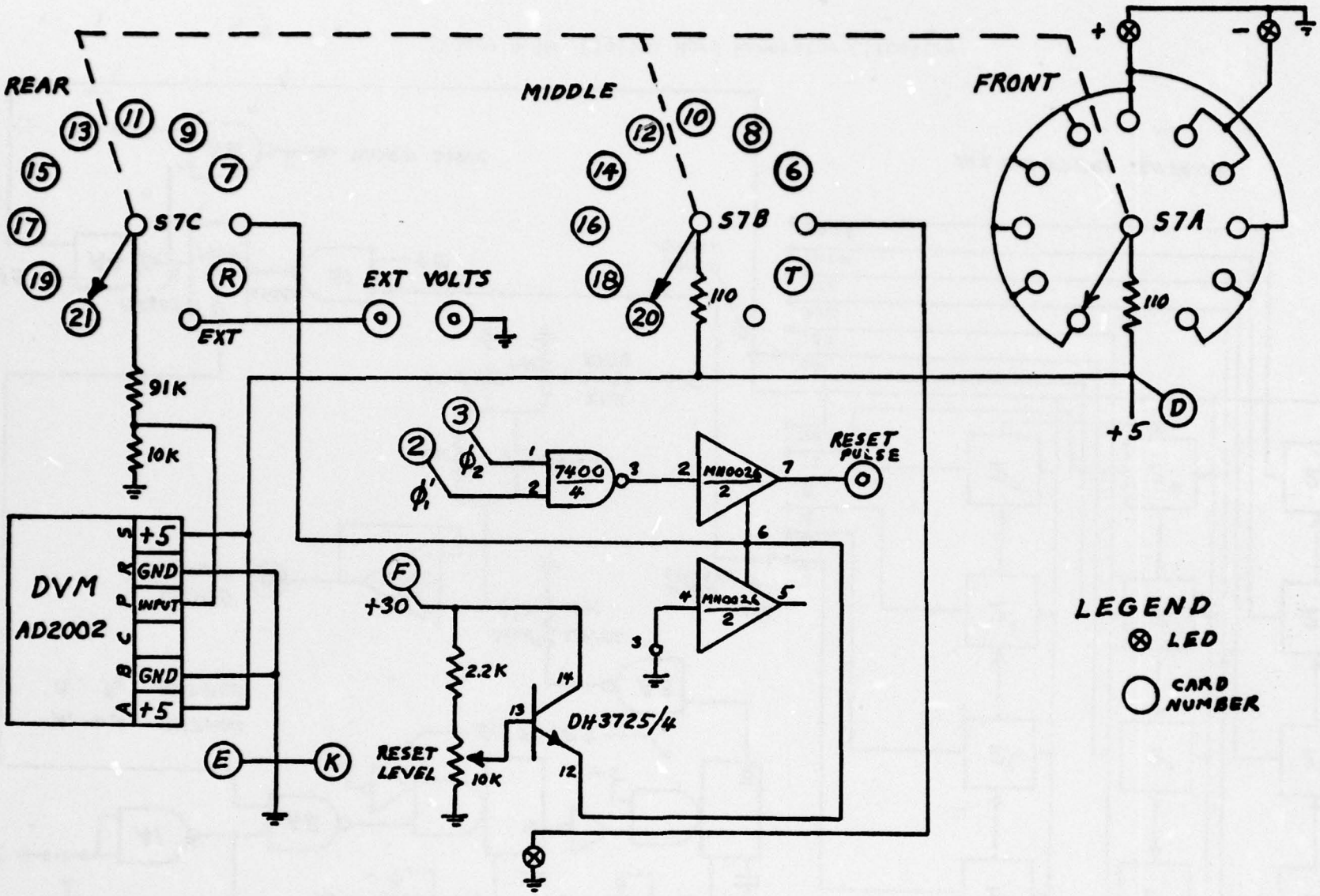


Figure 4.11 DVM Monitor and Reset Pulse Circuitry

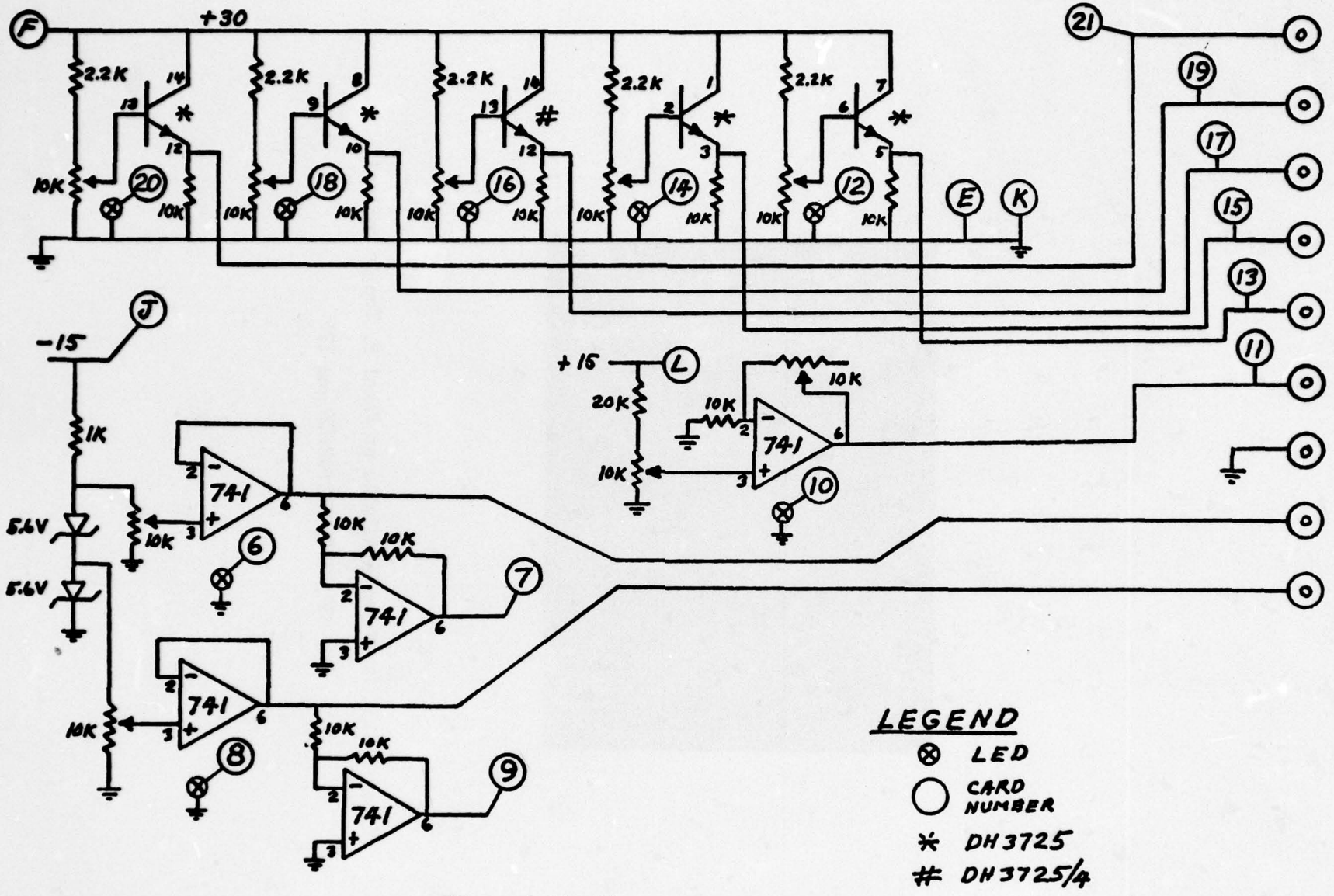


Figure 4.12 Bias Supply Circuitry

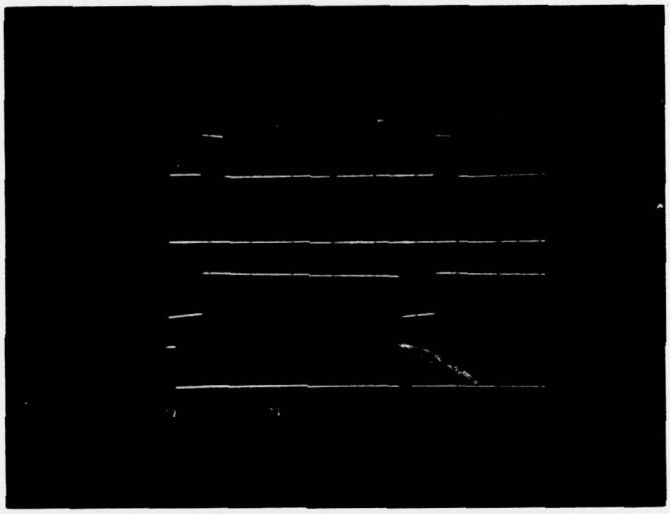


Figure 4.13. Waveforms available at Panel 2. Top to bottom:
INT PRF, SET, INTEGRATE and ITP

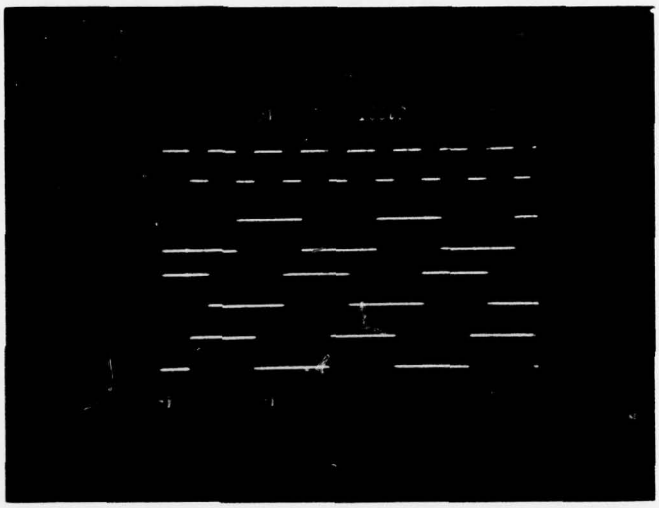
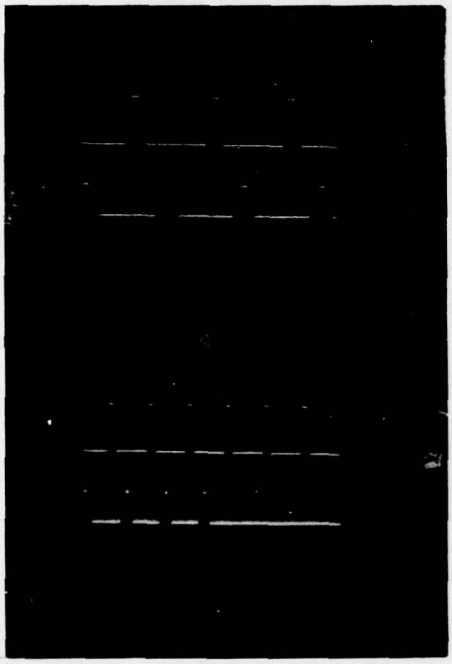


Figure 4.14. Master Clock and overlapping phase voltage waveforms.
Top to bottom: MC, $\phi_1(s)$, $\phi_2(s)$ and $\phi_3(s)$



Reset pulse

4 bit word

2 volts/div, 1 usec/div

Reset Pulse

4 bit word

2 volts/div, 2 usec/div

Figure 4.15 Reset pulse and 4 bit word output of word generator

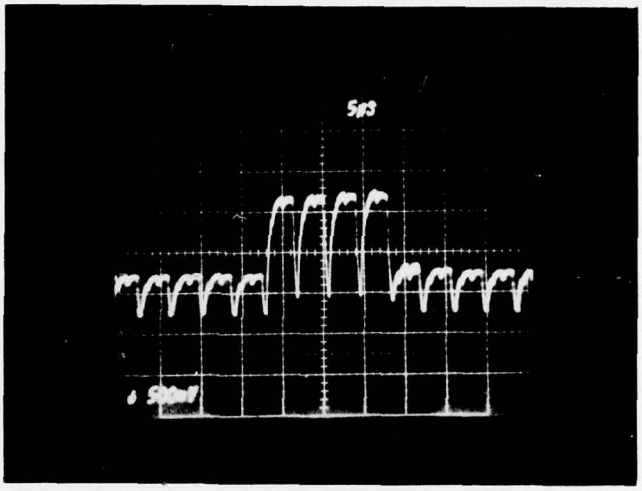


Figure 4.16. CCD output with 4 bit word input

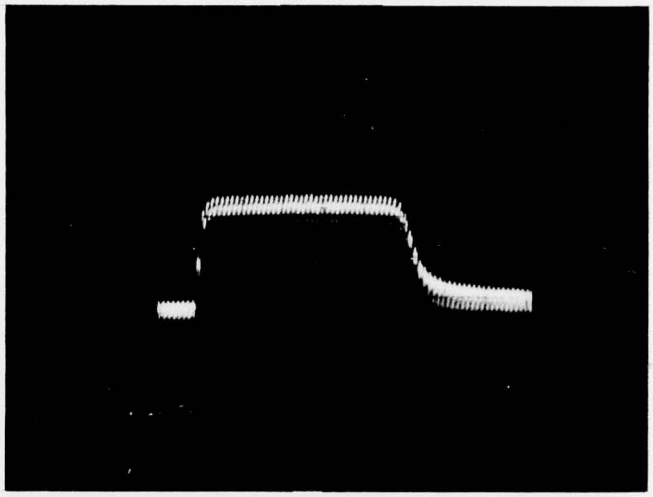


Figure 4.17a

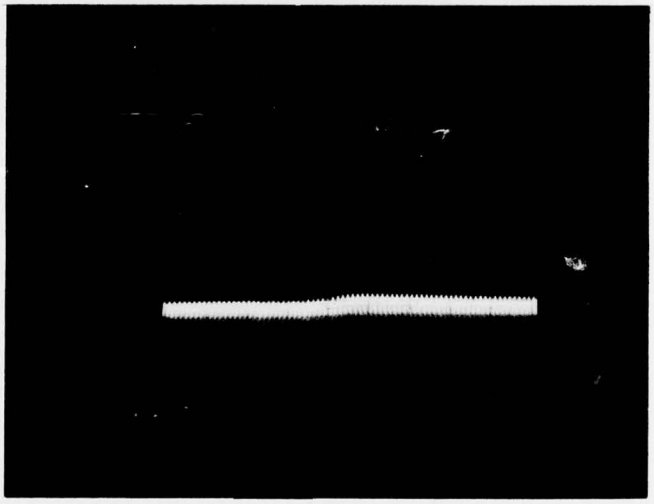


Figure 4.17b

Figure 4.17. CCD output using black body input (a) illuminated (b) non-illuminated

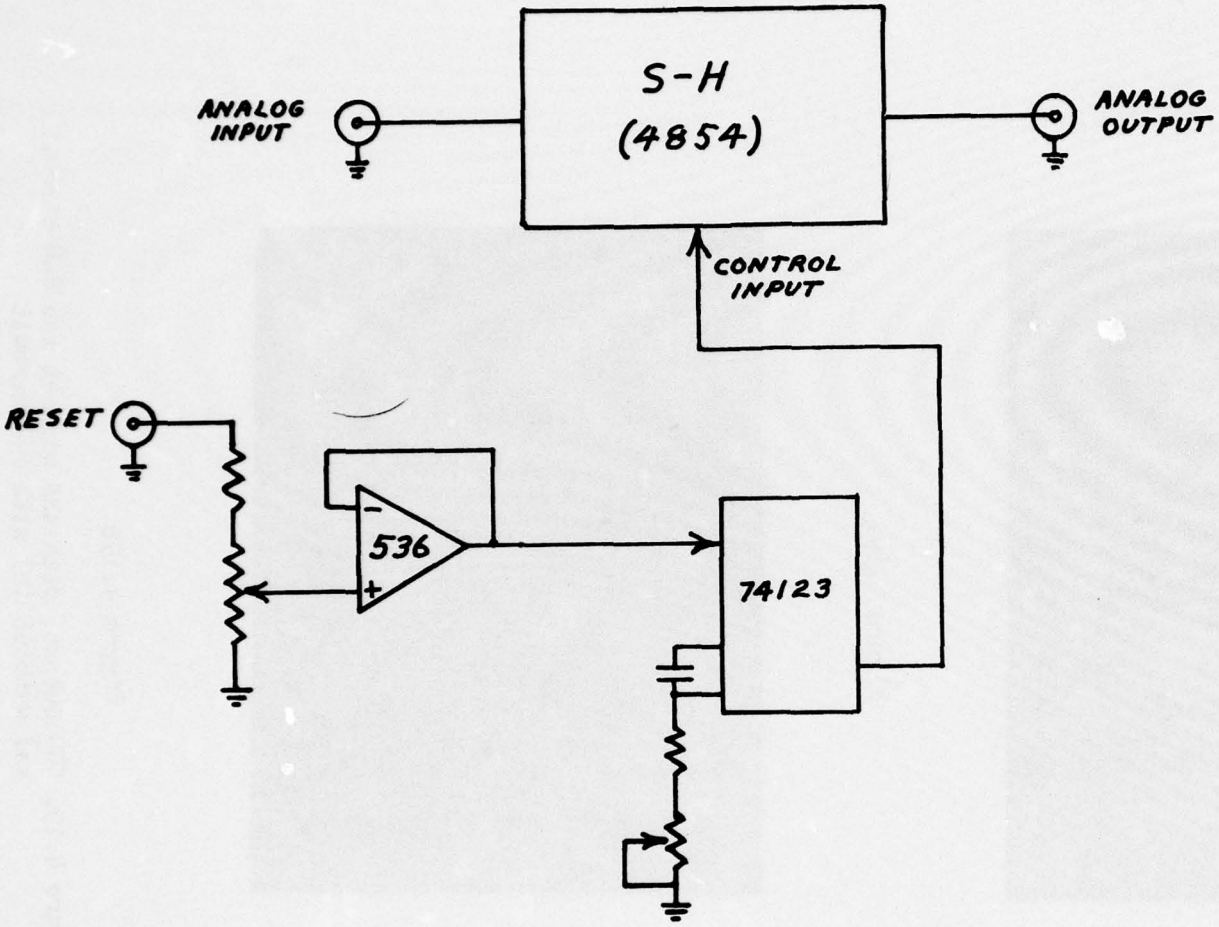


Figure 4.18 Sample-Hold circuit for noise reduction

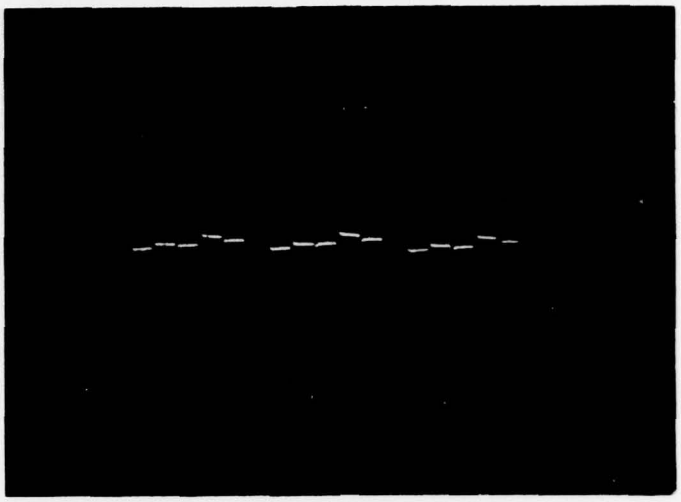


Figure 4.19a

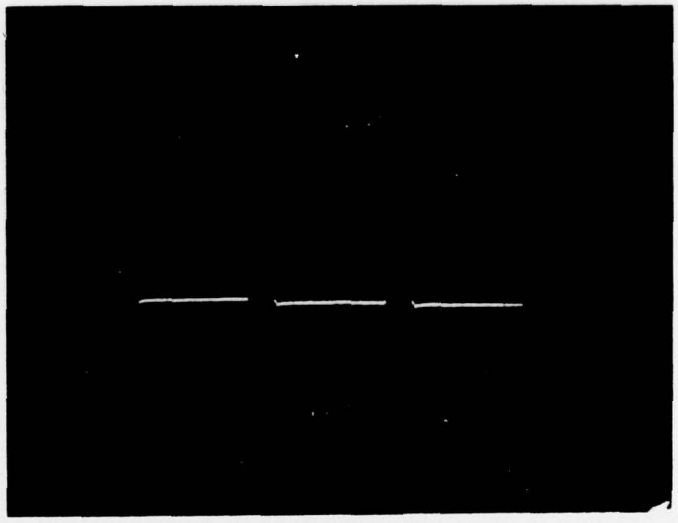


Figure 4.19b

Figure 4.19. CCD output, with and without the S_H circuit
(a) without (b) with S_H circuit

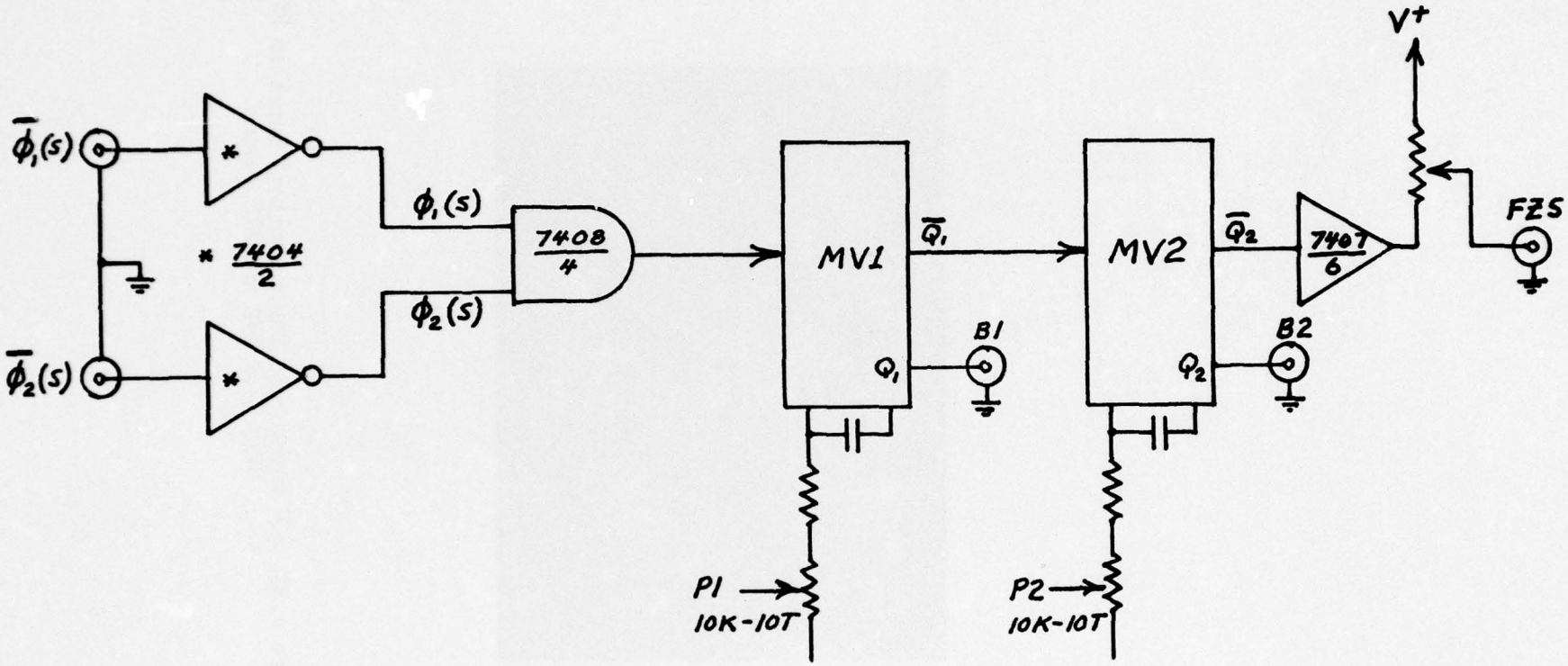


Figure 4.20 Fat zero circuitry, FZS, for the vidicon mode of operation

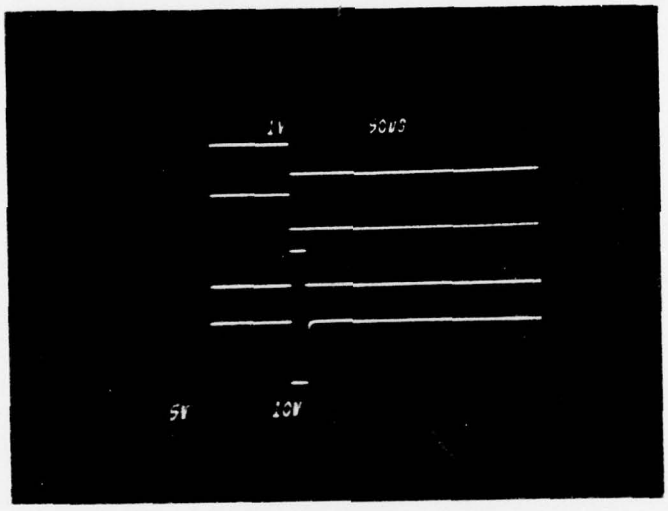


Figure 4.21. FZS waveforms. Top to bottom: input to MV1, Q of MV1, Q of MV2 and FZS output

Figure 4.22a. CCD output without fat zero or signal input showing dark current

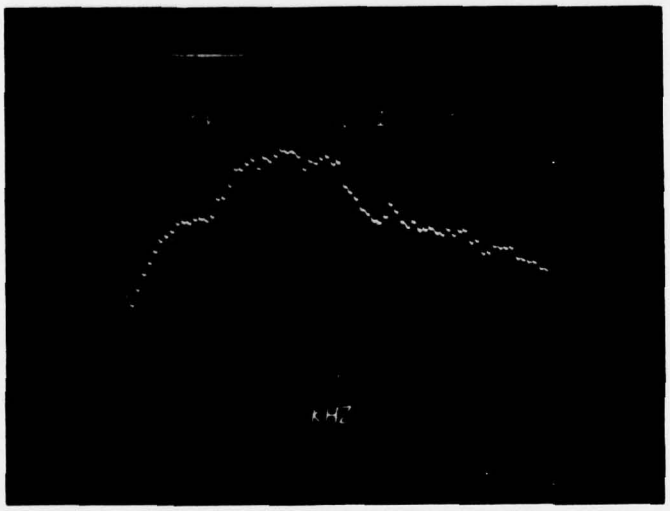


Figure 4.22b. CCD output with input signal and fat zero and dark current

Figure 4.22. CCD output, with and without input signal, using the S_H and FZS circuitry

PERSONNEL

A list of the scientists and engineers who contributed to the work reported is given below:

B. L. Cochrun, Professor of Electrical Engineering
Principal Investigator

R. Lawler, Undergraduate student

R. Aylward, Graduate student

J. Blacquier, Technician

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